# 3030 RF Digitizer PXI Module



# Operating Manual

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# About this manual

This manual applies to instruments with software issues of 2.0 and higher.

This manual explains how to set up and configure an Aeroflex 3030 RF digitizer PXI module. Where necessary, it refers you to the appropriate installation documents that are supplied with the module.

This manual provides information about how to configure the module as a stand-alone device. However, one of the advantages of Aeroflex 3000 Series PXI modules is their ability to form versatile test instruments, when used with other such modules and running 3000 Series application software.

*Getting Started with afDigitizer* (supplied on the CD-ROM that accompanies each module (see Associated documentation)) explains how to set up and configure a 3030 Series RF digitizer with a 3010 Series RF synthesizer module to form a high performance digitizer instrument. Using the digitizer soft front panel and/or dll or COM object supplied, the modules form an instrument that provides the functionality and performance of an integrated, highly-specified RF digitizer, but with the adaptability to satisfy a diverse range of test or measurement requirements.

# Intended audience

Users who need to install and configure the 3030 RF digitizer to down-convert and digitize RF signals.

This manual is intended for first-time users, to provide familiarity with basic operation. Programming is not covered in this document but is documented fully in the help files that accompany the drivers and associated software on the CD-ROM.

# Driver version

This PXI RF module is designed to be used with the latest software driver version supplied on the Aeroflex 3000 Series PXI Modules CD-ROM part no. 46886/028. Operation with earlier versions of driver software may not be supported.

# Structure

# Associated documentation

The following documentation covers specific aspects of this equipment:

| | | |
|---|---|---|
| **PXI Modules CD-ROM** | Part no. 46886/028 | Compilation containing soft front panels, drivers, application software, data sheets, getting started and operating manuals for this and other modules in the 3000 Series. |
| **3000 Series PXI Modules Common Installation Guide** | Part no. 46882/663 | Detailed information on installing modules into a rack, external connections, powering up and installing drivers. |
| **3000 Series PXI Modules Installation Guide for Chassis** | Part no. 46882/667 | Explains how to set up a populated chassis ready for use. |
| **PXI Studio User Guide** | Part no: 46892/809 | Setting up and using the universal PXI application for system configuration and operation. |
| **Getting Started with afDigitizer** | Part no. 46892/676 | Setting up and using the RF digitizer application for the 3010 Series and 3030 Series modules. |

# Preface

## The PXI concept

VXI and GPIB systems meet the specific needs of instrumentation users but are often too large and expensive for mainstream applications. PC-based instrumentation may cost less but cannot meet the environmental and operational requirements of many systems.

PXI (PCI Extensions for Instrumentation) is based on CompactPCI, itself based on the PCI standard. PCI was designed for desktop machines but CompactPCI was designed for industrial applications, and features a rugged Eurocard format with easy insertion and removal. PXI adds to the CompactPCI specification by defining system-level specifications for timing, synchronization, cooling, environmental testing, and software. While PXI extends CompactPCI, it also maintains complete interoperability so that you can use any CompactPCI-compliant product in a PXI system and vice versa. PXI also makes use of Windows software, VXI timing and triggering, and VXIplug&play instrument drivers to provide powerful and affordable systems.

# Abbreviations/acronyms

| | |
|---|---|
| ACPR | Adjacent Channel Power Ratio |
| ADC | Analog-to-Digital Converter |
| AM | Amplitude Modulation |
| ARB | Arbitrary Waveform Generator |
| CW | Continuous Wave |
| DAC | Digital-to-Analog Converter |
| dB | Decibels |
| dBc | Decibels relative to the carrier level |
| dBm | Decibels relative to 1 mW |
| FFT | Fast Fourier Transform |
| FM | Frequency Modulation |
| FPGA | Field Programmable Gate Array |
| GND | Ground |
| LO | Local Oscillator |
| LVDS | Low-Voltage Differential Signaling |
| PCI | Peripheral Component Interconnect |
| Pk-Pk | Peak-to-Peak |
| PXI | PCI eXtensions for Instrumentation |
| RF | Radio Frequency |
| RMS | Root Mean Square |
| SCSI | Small Computer Serial Interface |

| | |
|---|---|
| SFP | Soft Front Panel |
| SMA | SubMiniature version A (connector) |
| TRIG | Trigger |
| TTL | Transistor-Transistor Logic |
| UUT | Unit Under Test |
| VCO | Voltage-Controlled Oscillator |
| VSWR | Voltage Standing-Wave Ratio |
| VXI | VMEbus Extension for Instrumentation |

# Chapter 1 GENERAL INFORMATION



## Introduction

Welcome to the operating manual for the 3030 RF Digitizer PXI module.

The 3030, when used with a 3010 Series PXI RF synthesizer module, forms a compact RF digitizer that occupies only three slots in a 3U PXI chassis.

## Applications

The 3030 down-converts and digitizes RF signals. It converts an analog RF waveform presented at its RF port into a series of amplitude- and phase-corrected digital IF or IQ data pairs at its LVDS port. Software supplied with the module allows for spectrum analysis of the digitized signals.

The 3030 can be used in RF test and measurement systems used in development or manufacturing. Applications span all areas of UHF radio communications.

## Wide frequency coverage

The 3030 provides continuous frequency coverage from 330 MHz to 3 GHz. A linear single-stage down converter frequency converts to an IF centered on 46.08 MHz.

## Input range and accuracy

Input level control is provided by electronic switched attenuation, which helps to maximize the usable dynamic range. Good level accuracy and repeatability make the 3030 ideal for high-volume manufacturing.

## Wide bandwidth

The 3030 produces a 20 MHz wide digitized IF signal. Full-rate digital IF or decimated IQ data can be output via LVDS, useful for real-time emulation. Data can also be captured to internal memory and read over the PCI bus.

For narrowband signal analysis, the 3030 provides internal digital downconversion and decimation. Lowering the sample rate allows longer events to be captured. The 3030 contains digital resampling filters that allow you to set the sample rate, as well as numerous preset values associated with common digital communications standards.

## Signal routing

A configurable routing matrix provides flexibility in how you interconnect signals on the PXI backplane and the LVDS front-panel input. Predefined routing scenarios can be selected, or user-defined matrix settings stored and recalled.

**Triggering and synchronization**

The 3030 synchronizes to an external 10 MHz signal (generally supplied by the 3010/3011 RF Synthesizer). Triggering is external, from the PXI backplane or directly from the front-panel LVDS connector, or internal, from the internal timer or level trigger.

**Software**

The 3030 is supplied with a VXI PNP driver and soft front panel for use as a self-contained module. An instrument-level digitizer soft front panel, dll and COM object are also supplied: these allow you to use the 3030 together with a 3010 or 3011 RF Synthesizer. Refer to *Getting Started with afDigitizer* (part no. 46892/676), supplied on the PXI Modules CD-ROM part no. 46886/028. An FFT spectrum analyzer measurement suite is supplied, and optional signal analysis components are available to measure power, modulation quality and spectra to recognized standards.

*PXI Studio*, also supplied with the module, configures your PXI modules as logical instruments using an intuitive and powerful graphical interface. Currently, PXI Studio provides comprehensive signal generator, digitizer and spectrum analyzer applications and further development will provide analysis plugins to suit any modulation scheme.

*RF Investigator*, also supplied with the module, is an application that provides combined operation of all Aeroflex 3000 Series modules from a single user interface, especially useful for acceptance testing.

# Deliverable items

- 3030 RF Digitizer PXI module
- PXI Modules CD-ROM part no. 46886/028, containing soft front panels, drivers, application software, data sheets, getting started and operating manuals for this and other modules in the 3000 Series
- *3000 Series PXI Modules Common Installation Guide*, part no. 46882/663
- *3000 Series PXI Modules Installation Guide for Chassis*, part no. 46882/667
- SMA connector cable, part no. 43139/590 (2 off)

# Cleaning

Before commencing any cleaning, switch off the rack and disconnect it from the supply. You can wipe the front panel of the module using a soft cloth moistened in water, taking care not to wet the connectors. Do not use aerosol or liquid solvent cleaners.

# Putting into storage

If you put the module into storage, ensure that the following conditions are not exceeded:

Temperature range: $-20$ to $+70°C$ ($-4$ to $+158°F$)
Humidity: 5 to 93%, non-condensing

# Chapter 2 INSTALLATION

WARNING

## Initial visual inspection

Refer to the 3000 Series Common Installation Guide 46882/663.

CAUTION

## Handling precautions

Refer to the 3000 Series Common Installation Guide 46882/663.

## Hardware installation

### Installing the module into the PXI chassis

Refer to the 3000 Series Common Installation Guide 46882/663 and Installation Guide for Chassis 46882/667.

# Connector care and maintenance

## How to connect and torque an SMA connector

1   First, ensure that the mating halves of the connector are correctly aligned.

2   Next, engage the threads of the nut and tighten it by hand, ensuring that the mating halves do not move relative to each other.

3   Then use a torque spanner to tighten the connector, in order to ensure consistent matching and to avoid mechanical stress.

> Torque settings for connectors are:

> 0.56 Nm test torque (development use, semi-permanent installations)

> 1 Nm final torque (permanent installations)

Never use pliers to tighten connectors.

## Maintenance

### SMA

Clean connectors regularly, using a cotton bud dipped in isopropyl alcohol.  Wipe within the connector cavity, then use a dry cotton bud to finish off.  Check for any deposits.

Do not use other cleaners, as they can cause damage to the plastic insulators within the connectors.
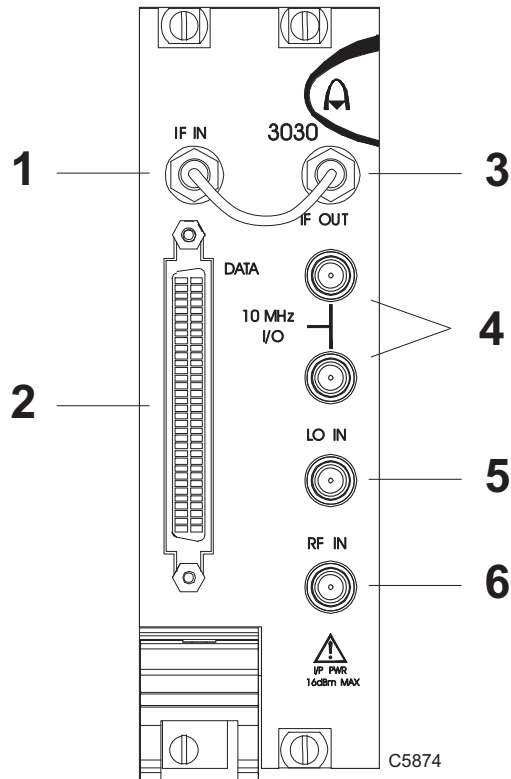
Cap unused connectors.

### PCI

Protect PCI connector pins by keeping modules in their original packing when not fitted in the rack.

# Chapter 3 OPERATION

# Front-panel connectors



*Fig. 3-1  3030 front panel*

1  IF IN  46.08 MHz input, −15 to +5 dBm for full-scale digitizer.  SMA socket, 50 Ω.

2  DATA  68-way SCSI connector for LVDS data I/O. See Appendix A for details.

3  IF OUT  46.08 MHz, nominally −5 dB relative to RF input, 0 dB attenuation selected.  SMA socket, 50 Ω.

4  10 MHz I/O  Two SMA I/O sockets in parallel.

   **Input**
   Frequency standard input for sampling clock.  50 Ω.  0.4 to 4 V pk-pk.

   **Output**
   Link-through from input.

5  LO IN  1.5 to 3 GHz, nominally 0 dBm.  SMA socket, 50 Ω.

6  RF IN  16 dBm max, 0 dB input atten.  SMA socket, 50 Ω.

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**CAUTION**

**Maximum safe powers**
 RF input: **+16 dBm** continuous (0 dB input attenuation)
 IF input: **+10 dBm** (0 dB IF attenuation)

# Soft front panel (af3030_sfp)

The soft front panel provides a graphical interface for operating the module. It is intended for testing and diagnosing, for demonstration and training, and for basic operation of the module. It represents most of the functions available in the instrument driver. It is not however a comprehensive application suitable for measurements; for this, use the afDigitizer DLL or afcomDigitizer COM object.

## Installation

The soft front panel is installed during the driver installation process (refer to the 3000 Series PXI Modules Common Installation Guide, part no. 46882/663).

Open the *AF3030_sfp.exe* file: this is in the *C:\VXIPNP\WinNT\af3030\* directory on a Windows NT machine, for example. It is also accessible from the Windows Start menu under *Programs\Aeroflex\PXI Module Front Panels\AF3030 Front Panel*. The soft front panel, similar to that in Fig. 3-2, is displayed.

## Detailed help information

Soft front panel controls are all available as driver export functions unless noted otherwise, and are documented in the help files. This operating manual provides an overview of the facilities that the module provides and summarizes its operation; however, refer to the help files for detailed descriptions of functions together with their parameter lists and return values.
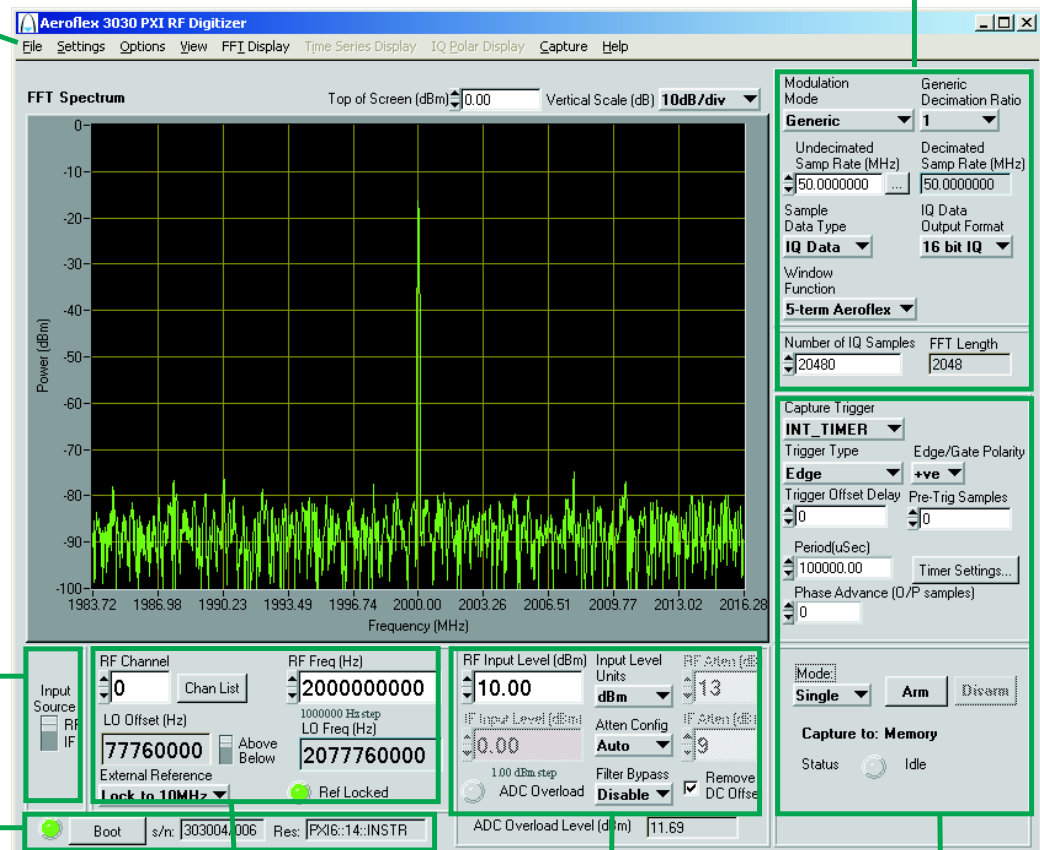
**Menu bar**

**IF/IQ data format**

**Input source**

**RF tuning**

**Input conditioning**

**Boot**

**Acquisition & triggering**



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*Fig. 3-2  3030 soft front panel*

# Soft front panel controls

## Menu bar

### File

**Save Captured Data (as <u>A</u>SCII file)…** captures the 16-bit sample data into the specified ASCII file.

**Save Captured Data (as <u>B</u>inary file)…** captures the 16-bit sample data into the specified binary file.

Click **<u>E</u>xit** to close the application.

### Settings

**<u>L</u>oad** and **Sa<u>v</u>e** allow you to load and save soft front panel configurations from and to your preferred locations.  If you did not change the default location when installing the software, it is *C:\VXIPNP\WinNT\af3030\settings*, and configurations are saved as *.ini* files.

> You can edit, copy and paste settings files as required; for example, you may want to save only a new routing setup without changing other parameters.  Edit the saved *.ini* file using a text editor (for example, Notepad) to remove unwanted parameters.  Ensure only that you do not delete the General (VendorID, DeviceID) and Version (Major/Minor) parameters.  Save the changed file.  When the settings file is next loaded, the configuration of the soft front panel changes to match the parameters remaining in the settings file.

**<u>D</u>irectories** lets you choose the location for your front-panel configuration settings.

**LVDS** allows you to set each LVDS <u>D</u>ata, <u>A</u>uxiliary and <u>M</u>arker mode for input, output or tri-state (default) operation.

- To use Spare 0 as a trigger input, set LVDS <u>D</u>ata to <u>I</u>nput.  Spare 0 is controlled by LVDS <u>D</u>ata Mode.

- To use an auxiliary bit as a trigger input, set LVDS <u>A</u>uxiliary to <u>I</u>nput

- To use a marker bit as a trigger input, set LVDS <u>M</u>arker to <u>I</u>nput.

- **IF Data Position** places 14-bit IF data in either the upper 14 bits of a 16-bit word (the lower two bits are padded with 0s) or lower 14 bits of a 16-bit word (upper two bits are sign extended), as required by the processing software.

**Routing Scenarios** allows you to select a predefined routing matrix connection.  A tick against the scenario's title shows that it is selected.

Selecting or removing a routing scenario affects only the connections specific to that scenario, and does not change any other routing connections.  However, changing the routing matrix connections of any scenario invalidates that scenario.

**Routing <u>M</u>atrix** displays a matrix that provides interconnection between input and output signals on the PXI backplane bus and the DATA connector, as shown diagrammatically in Fig. 3-3. This provides great flexibility in how you can route signals between modules.
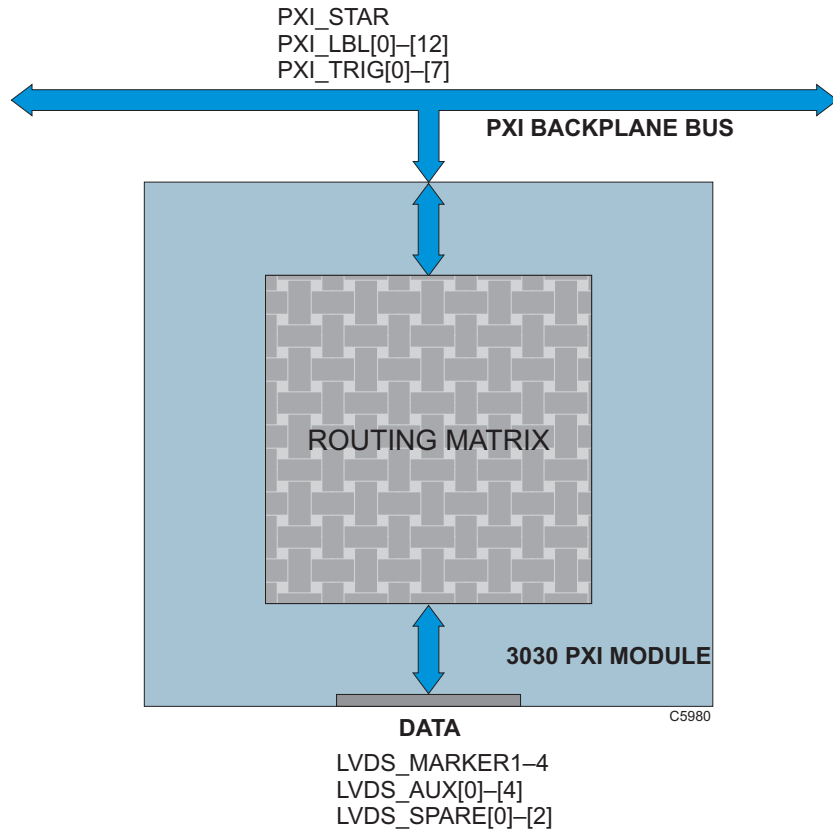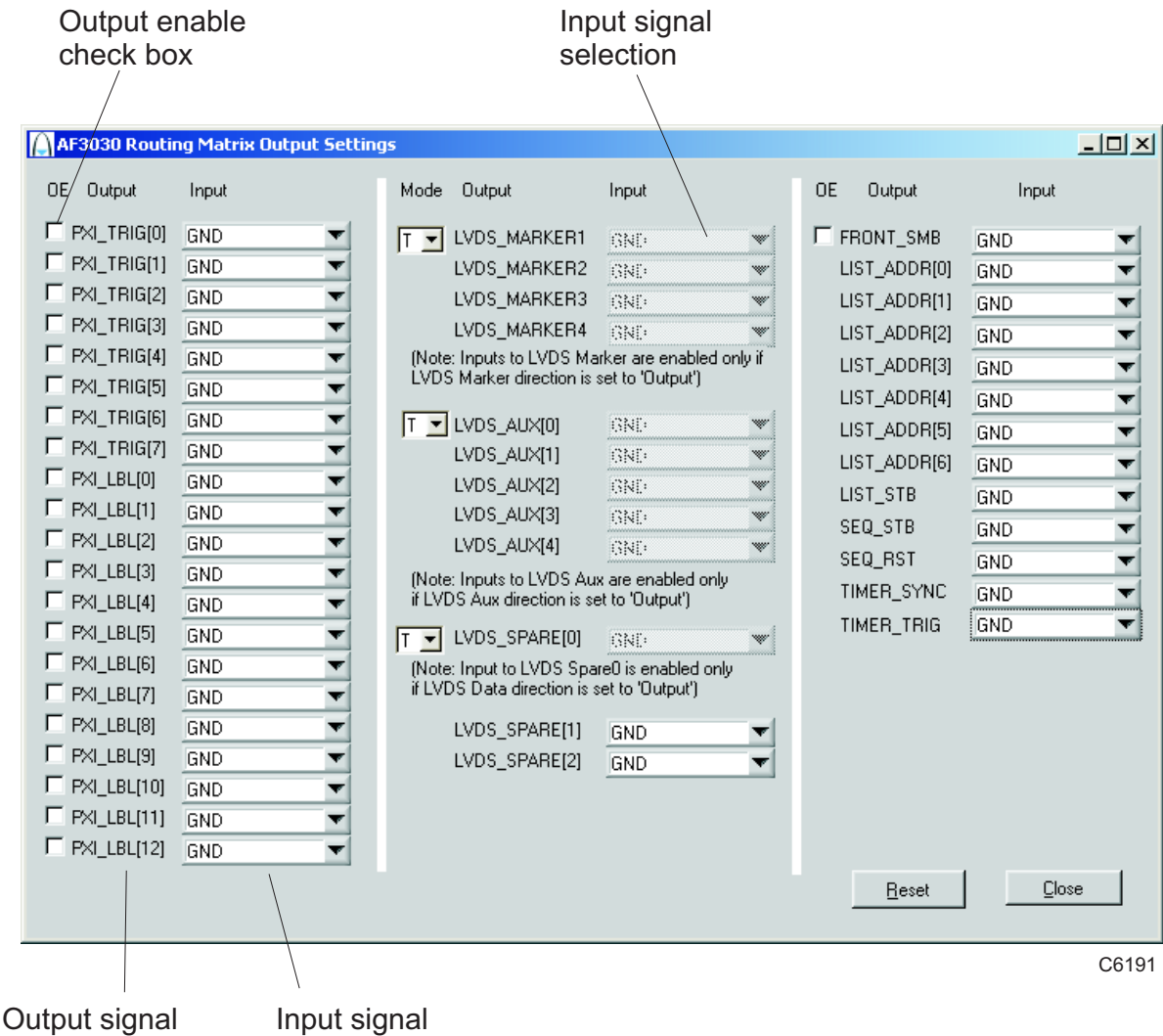


*Fig. 3-3  Routing matrix in 3030*

Use the matrix (Fig. 3-4) to interconnect signals. Output signals form the body of the matrix. Select appropriate input signals from the drop-down menus under each down-arrow to create the interconnections.

Check the boxes to enable the outputs and select the appropriate LVDS mode.

**Reset** connects all input signals to GND and disables the outputs (LVDS outputs go tri-state). This is the default state.

When operating the 3030 in default digitizer mode (routing matrix reset), all necessary input, output and trigger signals are available on front-panel LVDS and SMA connectors and there is no need to configure the matrix. If you need to set up particular signal routings, you can define these using the drop-down menus on the matrix and save them using the **Load** and **Save** commands in **Settings**, or use **Routing Scenarios** to access pre-set alternative routings, or contact Aeroflex if you need assistance in defining particular routing requirements.

Output enable
check box

Input signal
selection



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Output signal    Input signal

*Fig. 3-4  Routing matrix inputs and outputs*

**Optimization** allows you to choose how the 3030 compensates for the effect of temperature changes and RF frequency response.

Auto Temperature Optimization (default) monitors the temperature of the module at regular intervals and adjusts the correction figure for the current temperature. You can turn this off if it might interfere with a time-critical measurement.

Optimize Temperature Correction forces an immediate update, after which the timer starts a new interval.

Auto Flatness Mode compensates for the slope of the RF response, and may be needed for measurements taken over a wide bandwidth. It applies compensation to 'flatten' the response over the chosen bandwidth. The change in RF level due to RF response may not be significant for narrow-bandwidth measurements, which should be taken into account as auto flatness mode compensation may slow measurement time considerably. Default is 'off'.

## Options

Allows you to enable or disable additional instrument options if you have the appropriate password (available from the Aeroflex sales desk).  Click **Edit…** to display the options screen (Fig. 3-5).
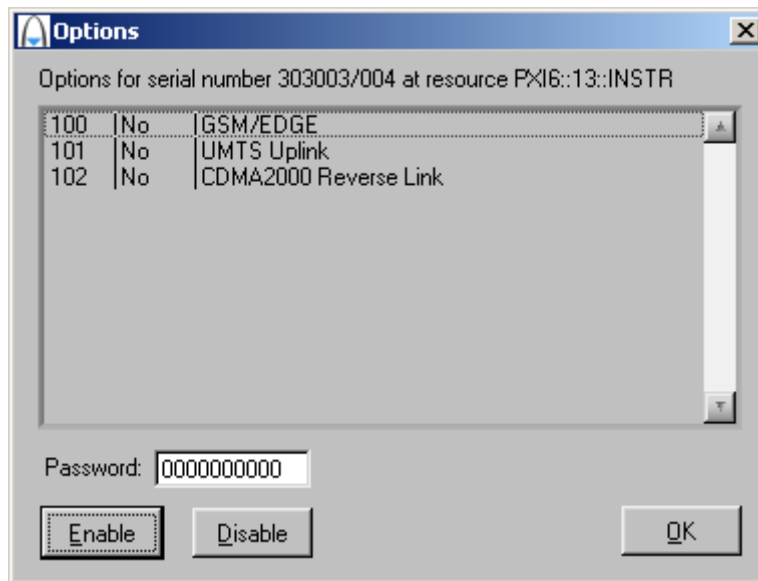


*Fig. 3-5  Options screen*

Disabled options are shown grayed out.  To enable an option, enter the appropriate password. Click **Enable**.  The enabled option is shown highlighted in green.  Click **OK**.

## View

Allows you to view results in different formats.

**View FFT** (default) displays a single graph showing power versus frequency. The default span is 66% of full span. You can modify the top of screen reference power (dBm) and the vertical scaling from (dB/div). Select other display settings from FFT Display.

**View Time Series** displays two graphs showing I and Q magnitude (in IQ mode) or IF magnitude (in IF mode) versus sample number. Sample Start and Sample End let you change the start and stop time of samples, allowing you to 'zoom in' on data. Select other display settings from Time Series Display.

**View IQ Polar** presents I and Q data as a polar response. Select other display settings from IQ Polar Display.

**View Numeric Data** displays IQ or IF data that can be placed alongside either the FFT or Time Series views. Numeric data representing the values of I and Q capture data is displayed as I first, followed by Q. Use the scroll bar to inspect long sample records.

## FFT Display

This menu is enabled only when View\View FFT is selected. It allows you to hide/display the graticule and save the dB levels of the trace as a *.txt* or other file.

**Graticule Visible** hides or displays the graticule.

The **Span** menu selects either Full or Truncated (approx. 66%) span. For example, with Modulation Mode set to UMTS and with a Decimation Ratio of 2, Full span is the full decimated bandwidth of the module — 30.72 MHz — and Truncated limits this to the module's bandwidth of 20 MHz, placing graticule lines at integer frequencies for easier reading.

**Save FFT Trace** saves the current FFT trace as a text file. The FFT trace is recorded as an array of dB values. The length of the array is displayed in the FFT Length field. The text file's location is defined in File Setup...

**File Setup…** allows you to select the filename and location for the FFT trace.

## T̲ime Series Display

When **View T̲ime Series** is selected, the T̲ime Series Display menu is enabled, allowing you view I and Q traces on two separate graphs or overlaid in different colors.

**G̲raticule Visible** hides or displays the graticule.

**IQ S̲eparate Graphs** displays separate graphs of Time Series (I) and Time Series (Q).  Both graphs are displayed with a common horizontal axis scaling (as set by Sample Start and Sample End).

**IQ O̲verlaid Graph** displays colored I and Q traces on a single graph; I is yellow and Q is green.

**F̲ull Width Sample View** adjusts the number of samples displayed in the graph to the number of samples captured.

**Y̲-axis Autoscale**: when selected, automatically sets the scaling of signal magnitude to the peak value.  When it is deselected, you can set the values manually using the Magnitude Min and Magnitude Max controls above the display.  The values of Magnitude Min and Magnitude Max apply to both I and Q when IQ S̲eparate Graphs is selected.

## IQ Polar Display

**G̲raticule Visible** hides or displays the graticule.

**A̲utoscale**, when selected, scales the I and Q signal magnitudes to the peak value.  When it is deselected, you can set the values manually using the IAxis Range (±) and QAxis Range (±) controls above the display.

# Capture

By default, 3030 captures data to the screen (**To <u>S</u>creen Only**), but you can also capture results to ASCII or binary files whilst continuing to display on screen (**To <u>A</u>SCII File and Screen**; **To <u>B</u>inary File and Screen**).

<u>**File Setup…**</u> opens a browser to define a file extension (default is *.txt*) and location for storing data. Files are saved as interleaved I/Q pairs (I followed by Q) or single IF data, depending on the setting of the Sample Data Type field.

- ASCII IQ file: I and Q values are on new lines, I value followed by Q value.
- Binary IQ file (16-bit mode): I and Q values are stored as 16-bit integers, I value followed by Q value.
  Binary IQ file (32-bit mode): I and Q values are stored as 32-bit integers, I value followed by Q value.

# Help

**Instrument Information** provides the module's PXI resource code and serial number, revision numbers for driver, FPGA and PCI, and its last calibration dates.

<u>**About**</u> provides the version and date of the soft front panel.

# Boot

Click **Boot** to initialize the module and view the Boot Resource window.  Resources available for initializing are shown in blue.

Select the 3030 you want to boot.

Boot default FPGA configuration box.
Check this.  Do not change the configuration unless you are advised otherwise.

EEPROM caching box.
Check this, so that when you boot a particular module for the first time, calibration data is read from the module and placed in the local cache that you define in the EEPROM Cache Path.  This initial boot time is of the order of 1 to 2 minutes.  Then check the EEPROM caching box at subsequent power-ups of this module to provide considerably faster boot times.  The EEPROM caching box is cleared at each power-down.

Click **OK**.  While you select the boot resource, the indicator is amber.  Once the module has initialized, the indicator changes to green in a few seconds.

If no calibration data is available, the driver returns a caution.  If this happens, return the module for calibration.

## s/n:

After the module initializes, this field displays its serial number.

## Res:

After the module initializes, this field displays its VISA resource string.

# Input source

Set this to RF or IF depending on which input is used (IF IN or RF IN).  Apply IF or RF signals to the appropriate input connector.  If the signal is RF, the module downconverts it and provides attenuator configuration and filtering options (see Input conditioning).  RF frequency settings/input level or IF input level controls are enabled, depending on which is selected, and unused controls are grayed out.

# RF tuning

## RF Channel

Sets the currently active channel of 0 to 127.

## Chan List

Click this to set up each of up to 128 channels (Fig. 3-6).  You can edit, copy and paste the settings to make setup quick and easy.



*Fig. 3-6  Edit all channel settings*

Edit the grid in the upper part of the screen by means of the fields in the lower part. Most fields (Frequency, LO Position, etc) are similar to those on the soft front panel. Edit each channel individually or by range for:

Channel
Freq (Hz)
LO Position
Atten Config
RF Level (dBm)
IF Level (dBm)
RF Atten (dB)
IF Atten (dB)
Period (μs/output samples

Select the channel to be edited either by changing the channel number on the panel or by clicking on the corresponding channel row in the channel list.

If you check the **Link channel selection to main panel** box, clicking on any parameter of a channel on this screen makes it become the active channel on the soft front panel.

Check the **Automatically set focus from grid select** box to make the associated field active when you click on a channel parameter in the grid.
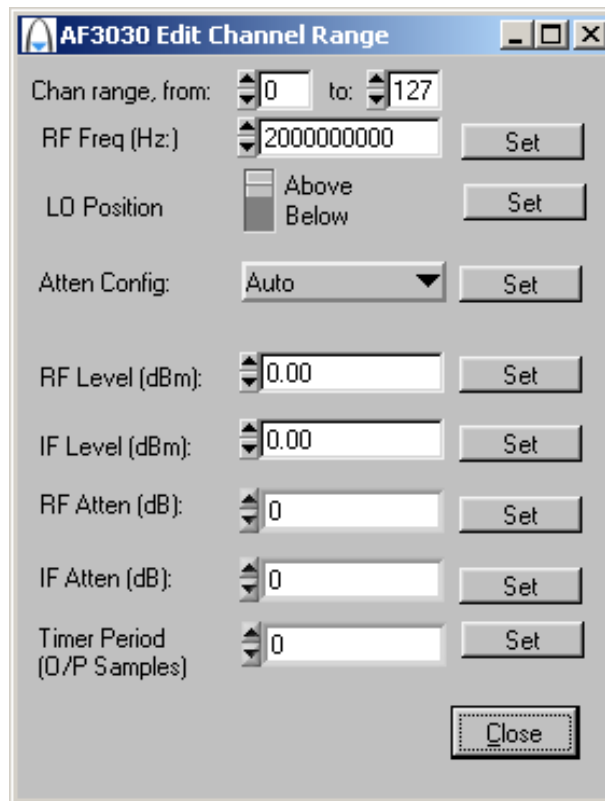
Check the **Use Channel Timers** box to use the active channel's period as the timer period. If the box is unchecked, the common timer period (measured in μs) applies to all channels. See Timer Settings.

Click **<u>T</u>imer…** to display the Timer Settings screen.

Click **Edit R<u>a</u>nge** to display the Edit Channel Range screen (Fig. 3-7), which lets you apply changes to a set of channels simultaneously, speeding up channel setup.

Define start and finish values for address numbers in the **Chan range, from:** and **to:** fields.

Insert values and click **Set** for each field.  You are asked to confirm each action.  When finished, click **<u>C</u>lose** to return to the Channel List screen.



*Fig. 3-7  Edit channel ranges*

## RF Freq (Hz)

This is the RF input frequency. This defines the center frequency of the FFT trace and selects appropriate correction values.

The module is tuned by setting the RF frequency and the LO offset direction (above or below). From these two values, the module calculates the LO frequency that must be applied to the LO input.

Set the output frequency using the up/down arrows or by entering the frequency in Hz or scientific (e) notation, in the range 330 MHz to 3.0 GHz.

## LO Offset (Hz)

Displays the local oscillator offset frequency in Hz.

Set the **Above/Below** switch to Above when the LO is higher in frequency than the RF (IF = LO–RF), and to Below when the LO is lower in frequency than the RF (IF = RF–LO).

## LO Freq

Shows the frequency to which a 3010/11 synthesizer module or other source should be set in order to provide the correct LO frequency for the 3030. If you are using a 3010/11, simply double-click on the field, copy the value, and paste it into the RF Frequency (Hz) field on the 3010/11's soft front panel.

## External Reference

**Lock to 10MHz** causes the ADC clock to lock to the 10 MHz reference connected to the 10 MHz I/O connector. **Free Run** causes the ADC clock to free run at the center of its range, at a nominal frequency of 61.44 MHz.

# Input conditioning

*You may find the block schematic diagram (Fig. 4-1) helpful in understanding these features.*

## RF Input Level

Set this to the <u>peak</u> level of the input RF signal to ensure the best dynamic range and signal-to-noise ratio.  Grayed out when Input Source is set to IF.

Set the RF input level using the up/down arrows or by entering the level, in the range −99.00 to +22.00 dBm (Atten Config = Auto) or −99.00 to +16.00 dBm (Atten Config = Auto IF or Manual).

*Note: when the RF input attenuation mimimum is set to 8 dB, the module can accept an input level of +22 dBm peak.  For any setting below 8 dB RF attenuation, the maximum safe input reduces to +16 dBm peak.*

## IF Input Level

Set this to the <u>peak</u> level of the input signal to ensure the best dynamic range and signal-to-noise ratio.  Grayed out when Input Source is set to RF.

Set the IF input level using the up/down arrows or by entering the level, in the range −99.00 to +17.00 dBm for full scale on the digitizer.

*Note: the maximum safe input with 0 dB IF attenuation is +10 dBm.*

**Step size:** double-click on the step value under the IF Input Level field to set up the size of RF and IF level step.

## RF Atten

Sets the RF attenuator value, which changes the input level to the mixer.  This value can only be adjusted manually if Atten Config is set to Manual or Auto IF.

Set the RF attenuator level using the up/down arrows or by entering the level, in the range 0 to +28 dB in 4 dB steps.

## IF Atten

Sets the IF attenuator value, which changes the input level to the ADC. This value can only be adjusted manually if Atten Config is set to Manual.

Set the IF attenuator level using the up/down arrows or by entering the level, in the range 0 to +35 dB in 1 dB steps.

## Input Level Dimensions

Establishes the measurement units as dBm, dBμV, dBmV, dBV, V or mW.

## Atten Config

| | |
|---|---|
| Auto | the RF input level set is used to optimize RF and IF attenuator gain settings automatically. |
| Auto IF | the IF input level set is used to optimize the IF attenuator settings, but you have manual control of RF attenuation. |
| Manual | ignores the RF input level you set, giving complete control over the settings of the RF and IF attenuators. |

## Filter Bypass

When enabled, causes the anti-aliasing filter to be bypassed, allowing signals outside its passband to reach the ADC. Level calibration is maintained. Allows you to observe spurii and other signals within the module's bandwidth that would otherwise be removed by the filter.

## ADC Overload (LED)

Indication is red if the ADC was overloaded during the last acquisition.

## ADC Overload Level

Indicates the RF/IF input level that could cause ADC Overload error. The overload level is displayed, but the input signal is clamped to the safe input level.

## Remove DC Offset

Removes the DC component from captured IF or IQ data. Removes DC components at the edge of the span at full and/or ½ sample rate.

*Note: if DC (but no signal) is present on the input, a sawtooth waveform is displayed on I and Q time series screens.*

# Acquisition & triggering

## Capture Trigger

Allows you to select the trigger source from a drop-down list:
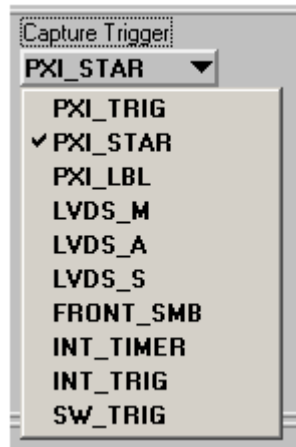


Software trigger

- **SW_TRIG**
  This is a non-triggered capture mode.  Click on **Start** to capture samples (defined by Number of Samples) when in Single/Repeat mode, without waiting for any external event.  Click **Stop** to end the capture.
  The indicator shows the status of the trigger or capture: green when waiting for a trigger or capturing, gray when idle.
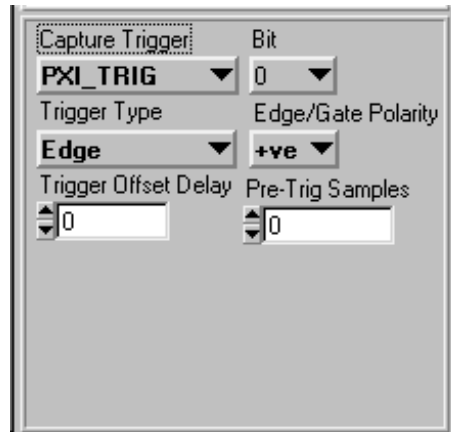
## Hardware triggers

The remaining triggers on the list are hardware triggers. When any of these are selected, triggering is dependent on trigger events, including the correct arming of the trigger.

The module ignores triggers that occur during the sample capture.

Refer to the help files for full details.

Most of the hardware triggers share a common triggering interface:

| | |
|---|---|
| Trigger Type | set to Edge or Gate |
| Edge/Gate Polarity | set +ve or –ve |
| Trigger Offset Delay | all hardware triggers can be delayed in the range $-10$ to $+2^9$ decimated samples. |



| | |
|---|---|
| Pre-Trig Samples (Edge trigger type) | sets the number of pre-trigger samples present in the captured data buffer. Increase this value to move the position of the trigger sample in the captured data further from the start. |



| | |
|---|---|
| Post-Trig Samples (Gate trigger type) | sets the number of post-trigger samples present in the captured data buffer. |
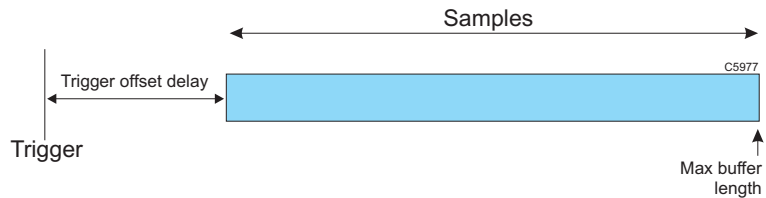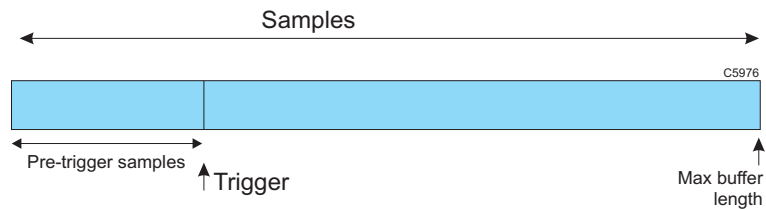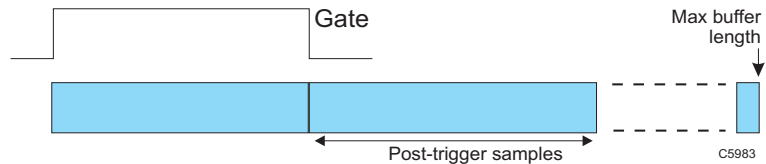
- **PXI_TRIG** [0–7]
  Takes its trigger input from any one of 8 bits of the PXI trigger bus that is common to all modules in the chassis.

- **PXI_STAR**
  Takes its trigger input from a module that has ST functionality and is fitted in PXI slot 2.

- **PXI_LBL** (Local Bus Left) [0–12]
  Takes its trigger input from the slot to the left of the 3030 (viewed from the front panel), using the PXI local bus. Choose from any of 13 bits for the trigger; this bus is common only to the 3030 and the module to its left.

- **LVDS_M** [1–4]
  Takes its trigger from any of four Marker bits on the DATA connector. Ensure that Settings/LVDS/Marker Mode is set to Input.

- **LVDS_A** [0–4]
  Takes its trigger from any of five Auxiliary input bits on the DATA connector. Ensure that Settings/LVDS/Auxiliary Mode is set to Input.

- **LVDS_S**
  Takes its trigger from the Spare 0 input bit on the LVDS data bus. Ensure that Settings/LVDS/Data Mode is set to Input. Because the data bus is set to receive when this trigger is used, it is not then possible to output data on the DATA connector.

- **INT_TIMER**
  Takes its trigger from the internal timer.  This timer trigger can also be routed to other modules using the routing matrix.  Similarly, this timer can be synchronized with the external signal connected to the TIMER_SYNC signal in the routing matrix.
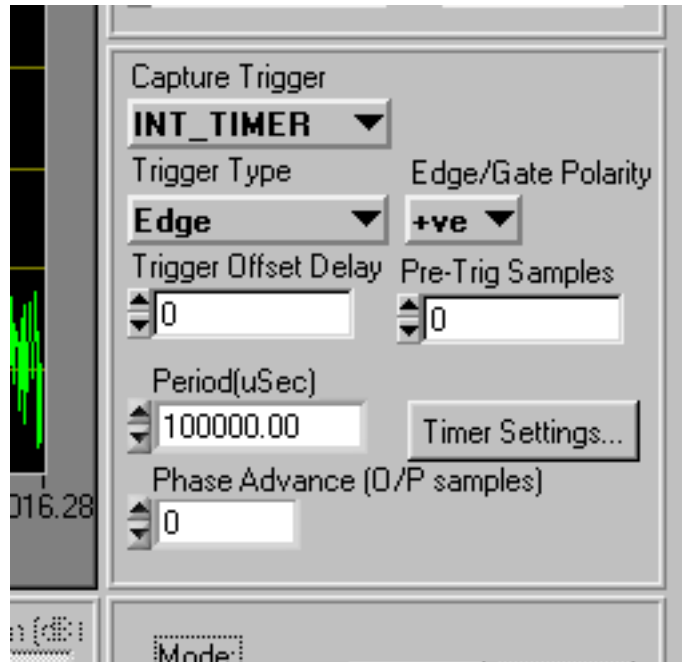
Click **Timer Settings…** to display the Timer Settings screen (Fig. 3-8).

*Fig. 3-8  Timer settings*

Channel Timer Mode

When checked, lets you use a different timer period for each channel.  The timer period is determined by the active channel's Period (see below), and applies while that channel is active.  This mode is useful in setting up variable dwell list mode.

The channel timer period is measured in number of output samples, so changes if the sample rate changes.  When the channel changes, the timer restarts, using the period set for that channel.
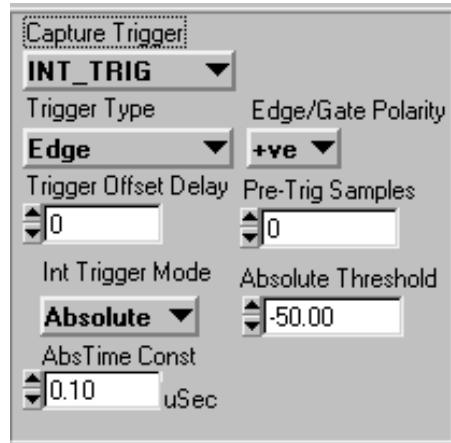
If Channel Timer Mode is disabled, the timer period becomes the common timer period, specified in μs.  This timer period stays the same irrespective of which channel is active, and does not restart when the channel changes.

| | |
|---|---|
| Period | Sets the period of the active channel (in number of output samples) if Channel Timer Mode is enabled.  Otherwise, sets the common timer period in µs.  Mark/space ratio in either mode is 50%. |
| Phase Advance | Adjusts the phase of the internal timer signal in multiples of the output sample clock period.  Allows you to synchronize the timer trigger with an external signal.  Not available if Channel Timer Mode is enabled. |
| Timer Arm | Arms the timer so that an external signal connected to TIMER_TRIG in the routing matrix triggers the timer (rising edge). |
| Timer Start | Starts the timer if it was stopped, otherwise ignored if the timer is already running.  Initial state of timer is 'High'. |
| Timer Stop | Stops the timer if it is running, and disarms the timer trigger. Once the timer is stopped, an external signal cannot start it without re-arming it. |

Settings for Period and Phase Advance (in common timer mode only) appear on the front panel as well as on the Timer Settings screen.

- **INT_TRIG**
  Takes its trigger from the internal level trigger.

Int Trigger Mode     Select the internal level trigger mode: Absolute/Relative

Absolute: the digitized signal is filtered using an absolute time constant.  An internal level trigger is generated when the level of this filtered signal exceeds the absolute level trigger threshold (specified in dBm).  The absolute time constant and level settings may affect the trigger delay.

Relative: the digitized signal is filtered using both a fast and a slow time constant.  For a step level change, the amplitude difference between the two resultant filtered signals produces a pulse, its duration and level determined by the difference between the fast and slow time constants.  The pulse is then compared with the 'relative threshold trigger level' to create the internal trigger.  Fig. 3-9 shows this.

When the relative threshold trigger level is entered as positive, the difference signal = (fast signal – slow signal). When relative threshold trigger level is entered as negative, the difference signal = (slow signal – fast signal).

Only +ve Trigger Edge/Gate Polarity is available when using relative mode.

AbsTime Const     Sets the time constant for the absolute level internal trigger.

Absolute Threshold     Sets the absolute threshold level in dB.

Relative Slow/Fast Time Const     Sets the slow and fast time constants used in relative internal trigger mode.

Relative Threshold     The threshold value (dBm) compared with the difference signal filtered using Relative Slow and Fast Time Constants.

*Fig. 3-9  Relative internal level trigger mode*

## Trigger mode and control

**Mode:**

Selects **Single**-shot or **Repeat** data capture.

Use with the **Start** and **Stop** buttons to initiate and stop data capture.

The indicator shows the status of the trigger or capture: green when waiting for a trigger or capturing, gray when idle.

# IF/IQ data format

## Sample Data Type

Select IQ or IF sample data type.

- IQ Sample Data: output sample rate is determined by the Modulation Mode and Decimation Ratio

- IF Sample Data: output sample rate is fixed at 61.44 MHz

## Modulation Mode

(IQ data format only) Sets the digital modulation mode:
Generic/UMTS/GSM/CDMA2000 1X/2319 Emulation.

The sample rate varies, depending upon modulation mode and decimation ratio:

- Generic: user-defined.  Use this mode to create or emulate any modulation scheme.
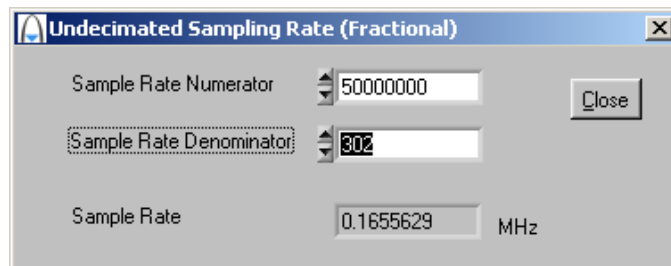
  Enter any Undecimated Sample Rate in the range 3750 Hz to 30.72 MHz (LVDS transfer) or 50 MHz (PCI transfer) with a Generic Decimation Ratio of 1.

  Alternatively, enter a different Generic Decimation Ratio and scale the Undecimated Sample Rate accordingly.

  The resultant sample rate is shown in the Decimated Sample Rate box.

  or

  define a fractional rate by setting the numerator and denominator.  Click on the button adjoining the Undecimated Sample Rate box to open the popup panel and enter a fractional sample rate:

Pre-defined rates:

- UMTS data mode: 61.44 MHz/$2^N$ (where N = 1 to 10)
- GSM resampled IQ data mode: 13 MHz/(3 * $2^N$), where N = 0 to 4 ($2^{(4-N)}$ times symbol rate of 13 MHz/48)
- CDMA2000 1X resampled IQ data mode: 9.8304/$2^N$, where N = 0 to 3 ($2^{(3-N)}$ times chip rate of 1.2288 MHz)
- 2319 emulation mode: 65.28/$2^N$, where N = 4 or 5.

## Decimation Ratio (Generic/GSM/UMTS/CDMA2000 X1/2319E)

(IQ data format only) Select a decimation ratio, dependent on the modulation mode:

| | |
|---|---|
| GENERIC | $2^n$ where n = 0 to 14 (max) |
| GSM | $2^n$ where n = 0 to 4 |
| UMTS | $2^n$ where n = 1 to 10 |
| CDMA2000 1X | $2^n$ where n = 0 to 3 |
| 2319E emulation | $2^n$ where n = 4, 5 |

See Data timing.

## Undecimated Samp Rate

Displays the internal undecimated sampling rate before division by the decimation ratio.

| | | |
|---|---|---|
| GENERIC | max 50.00 MHz (PCI transfer); max 30.72 MHz (LVDS transfer) | |
| UMTS | 61.44 MHz | = 3.84 MHz (3GPP chip rate) x 16 |
| GSM | 4.3333 (rec.) MHz | = 270.8333 (rec.) kHz (GSM bit rate) x 16 |
| CDMA2000 1X | 9.8304 MHz | = 1.2288 MHz (CDMA2000 chip rate) x 8 |
| 2319E | 65.28 MHz | = 3.84 MHz (3GPP chip rate) x 17 |
| IF | 61.44 MHz | |

# IQ Data Output Format

Select 16- or 32-bit, subject to the modulation mode and decimation ratio chosen.

**Sample rates**

| Modulation | Decimation ratio | IQ sample rate (Msymbol/s) | IQ data format |
|---|---|---|---|
| GENERIC | $2^n$ where n = 0 to 14 (max) | variable | 16 (when Output Sample Rate > 7.68 MHz ) 16/32 (when Output Sample Rate <= 7.68 MHz) |
| UMTS | 2 | 30.72 | 16 |
|  | 4 | 15.36 | 16 |
|  | 8 | 7.68 | 16/32 |
|  | 16 | 3.84 | 16/32 |
|  | 32 | 1.92 | 16/32 |
|  | 64 | 0.96 | 16/32 |
|  | 128 | 0.48 | 16/32 |
|  | 256 | 0.24 | 16/32 |
|  | 512 | 0.12 | 16/32 |
|  | 1024 | 0.06 | 16/32 |
| GSM | 1 | 4.33333 | 16/32 |
|  | 2 | 2.16666 | 16/32 |
|  | 4 | 1.08333 | 16/32 |
|  | 8 | 0.541667 | 16/32 |
|  | 16 | 0.270833 | 16/32 |
| CDMA2000 | 1 | 9.8304 | 16 |
|  | 2 | 4.9152 | 16 |
|  | 4 | 2.4576 | 16 |
|  | 8 | 1.2288 | 16/32 |
| 2319E | 16 | 4.08 | 16/32 |
|  | 32 | 2.04 | 16/32 |

## Window Function

Defines the window used by the FFT.  5-term Aeroflex gives good noise performance and side-lobe suppression at the expense of a wider main lobe, optimal for ACPR measurements.

## Decimated Samp Rate

Displays the result of the undecimated sampling rate divided by the decimation ratio.

## Number of Samples

Sets the sample size (number of samples to be captured), up to $32 \times 10^6$ IQ pairs with 32-bit storage, $64 \times 10^6$ IQ pairs with 16-bit storage, or $128 \times 10^6$ IF samples.

## FFT Length

Varies with number of IF/IQ samples set.  Minimum 16, maximum 2048.

# Driver export functions

On-line help and functional documentation for driver export functions are available on the CD-ROM supplied with your module.  They are installed onto your computer at the same time as the drivers.

## Driver installation folder

Find help and functional documentation in the driver installation folder on your computer. This is typically:

> *C:\vxipnp\winnt\af3030*

## Help

Within this folder are help files that provide detailed descriptions, parameter lists and return values for all available functions.  Help files are provided in three formats:

| | | |
|---|---|---|
| *af3030.doc* | 3030 function documentation | Text file |
| *af3030.hlp* | 3030 Visual BASIC function reference | Windows Help file format |
| *af3030_C.hlp* | 3030 C language function reference | |

We recommend that you use the C or Visual Basic formats, as these are easier to navigate.

The file opens at the Contents page:
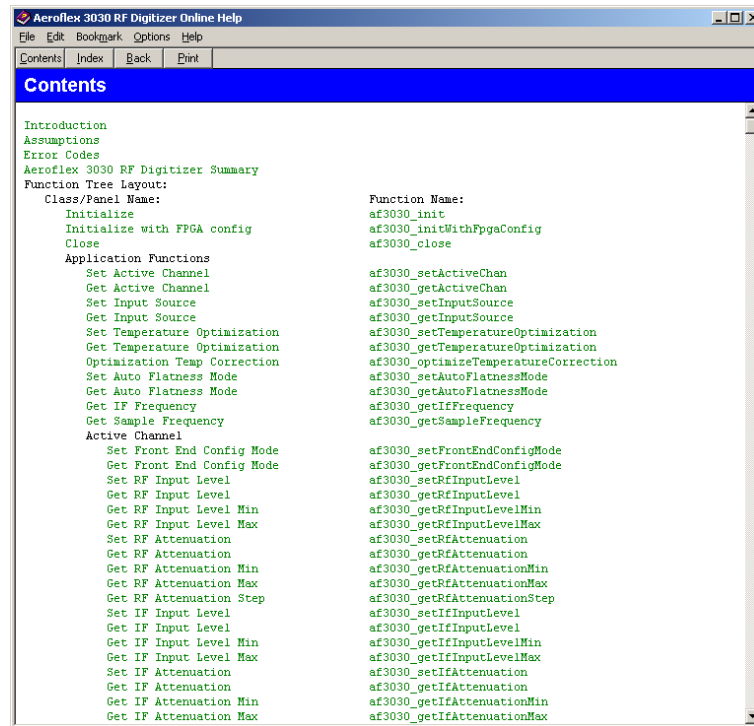


*Fig. 3-10  Online help contents — example*

Hyperlinks from here take you to

>Introduction

>Assumptions

>Error codes

>Functions listings

# Functions listings

Functions are grouped by type.  Click on the hyperlink for details of the function.  Each function has a description of its purpose, and may have a list of parameters and return values.
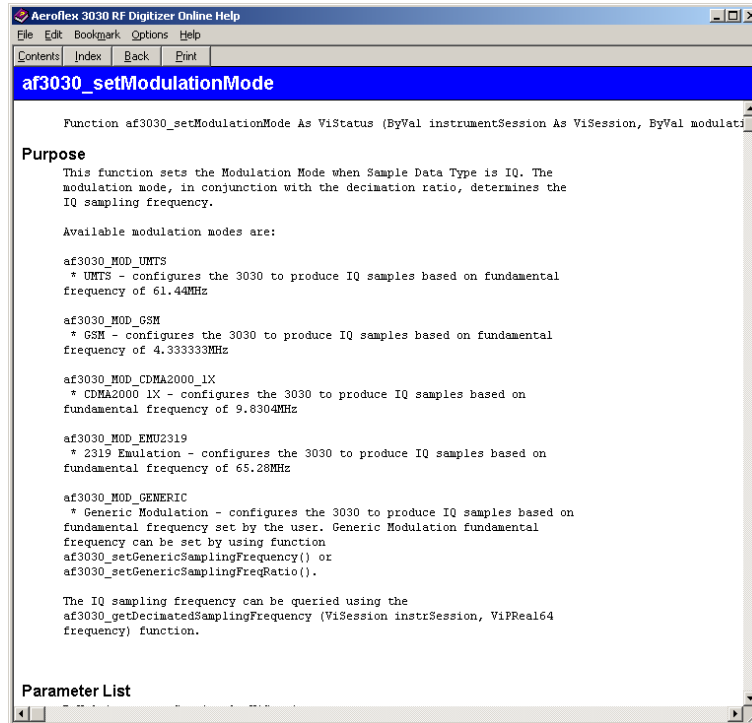


*Fig. 3-11  Function description — example*

# RF digitizer using 3010/3011 and 3030

Refer to *3000 Series PXI Modules Installation Guide for Chassis* (part no. 46882/667) and *Getting Started with afDigitizer* (part no. 46892/676), both supplied on the CD-ROM with the module, for detailed information on creating a fully functional RF digitizer using the 3030 and 3010/3011 together.  The afDigitizer soft front panel and associated afDigitizer dll and afcomDigitizer COM object combine the functions of the individual modules to provide a single interface with the appearance and functionality of an integrated instrument.

# Appendix A
# DATA connector and timing

The DATA connector is a 68-way female VHDCI-type LVDS (low-voltage differential signaling) interface.  It can be used to output data and associated control and timing signals.

The DATA connector is shown in Fig. A-1.  LVDS data conforms to ANSI/TIA/EIA-644.
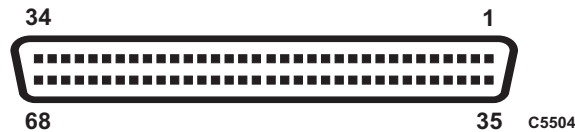


*Fig. A-1  DATA connector (looking onto front panel)*

The DATA interface provides:

- output of IF or IQ data
- input/output of triggering, List Mode and Timer signals.
- clock

The electrical level is LVDS: $V_{OH}$ typically 1.38 V, $V_{OL}$ typically 1.03 V

## Table A-1  DATA pin-out

| Contact | Function | Contact | Function |
|---------|----------|---------|----------|
| 1 | AUX0- | 35 | AUX0+ |
| 2 | AUX1− | 36 | AUX1+ |
| 3 | AUX2− | 37 | AUX2+ |
| 4 | SPARE1− | 38 | SPARE1+ |
| 5 | SPARE2− | 39 | SPARE2+ |
| 6 | CLK_IN− | 40 | CLK_IN+ |
| 7 | GND | 41 | GND |
| 8 | CLK_OUT− | 42 | CLK_OUT+ |
| 9 | D0− | 43 | D0+ |
| 10 | D1− | 44 | D1+ |
| 11 | D2− | 45 | D2+ |
| 12 | D3− | 46 | D3+ |
| 13 | D4− | 47 | D4+ |
| 14 | D5− | 48 | D5+ |
| 15 | D6− | 49 | D6+ |
| 16 | D7− | 50 | D7+ |
| 17 | D8− | 51 | D8+ |
| 18 | D9− | 52 | D9+ |
| 19 | D10− | 53 | D10+ |
| 20 | D11− | 54 | D11+ |
| 21 | D12− | 55 | D12+ |
| 22 | D13− | 56 | D13+ |
| 23 | D14− | 57 | D14+ |
| 24 | D15− | 58 | D15+ |
| 25 | IQSELECT_OUT− | 59 | IQSELECT_OUT+ |
| 26 | IQSELECT_IN− | 60 | I/QSELECT_IN+ |
| 27 | SPARE0− | 61 | SPARE0+ |
| 28 | GND | 62 | GND |
| 29 | MARKER1− | 63 | MARKER1+ |
| 30 | MARKER2− | 64 | MARKER2+ |
| 31 | MARKER3− | 65 | MARKER3+ |
| 32 | MARKER4− | 66 | MARKER4+ |
| 33 | AUX3− | 67 | AUX3+ |
| 34 | AUX4− | 68 | AUX4+ |

# Data format

The data output to the DATA interface is real-time. In resample mode, data is output using a 61.44 MHz clock but bursted to achieve the correct average sample rate.

| Sample DATA | Decimated IQ (also resampled IQ): |
|---|---|
| | 16-bit IQ, 2 x D[15:0], I followed by Q, D[0]=LSB. |
| | 32-bit IQ, 4 x D[15:0] in order I MSW, I LSW, Q MSW, Q LSW, D[0]=LSB. 32-bit data available only for decimate by 8 or more. |
| | IF data: there are two configurations: |
| | Upper 14 bits: D[15:2], D[2]=LSB (default mode) |
| | Lower 14 bits: D[13:0], D[0] = LSB, D[15:14] sign extended from D[13]. |
| IQSELECT_OUT | Determines if the data is I (IQSELECT_OUT=1) or Q (IQSELECT_OUT=0). |
| | Q is defined during the single clock period following IQSELECT_OUT going low. Thereafter, Q is indeterminate until IQSELECT_OUT goes positive to define a new IQ pair. |
| | IQSELECT_OUT=0 at all times in IF mode. |
| CLK+ | Data changes on the falling edge. |
| CLK− | Data changes on the rising edge. |

# Data timing

## Data transmission for generic modulation mode

In this mode, IQ data is resampled to produce IQ data in the range $30.72 \text{ MHz}/2^N$, where $N = 0$ to 13. . The timing relationships for the DATA interface is as shown in Fig. A-2. Note that the CLK_OUT signal is continuous and that the frequency of the clock remains fixed at 61.44 MHz. IQSELECT_OUT is toggled only when an IQ data pair is being transmitted. There is no integer relationship between the data rate and the clock frequency of 61.44 MHz. Therefore the number of clock cycles between IQSELECT_OUT being asserted varies.
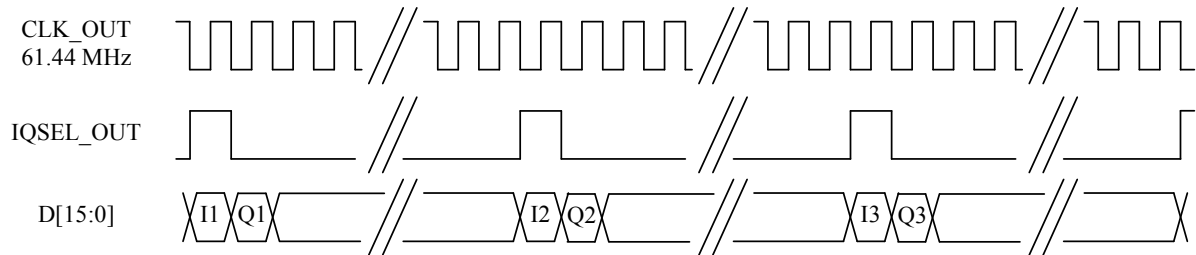


*Fig. A-2  DATA timing for generic modulation*

# Latency

The digitizer converts an analog RF waveform presented at its RF port into a series of digital IQ data pairs at its LVDS port. LVDS latency is the time taken for any given point on the input RF waveform to appear as an IQ data pair on the LVDS output. The table below gives examples of LVDS latency times for different IQ sample rates.

| Generic modulation (30.72 MHz) | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Decimation ratio | 1 | 2 | 4 | 8 | 16 | 32 | 64 | 128 | 256 | 512 |
| Output sample rate (MHz) | 30.72 | 15.36 | 7.68 | 3.84 | 1.92 | 0.96 | 0.48 | 0.24 | 0.12 | 0.06 |
| Total delay (µs) | 2.20 | 2.93 | 4.26 | 6.93 | 12.01 | 22.17 | 42.48 | 83.10 | 164.35 | 326.85 |

| Generic modulation (23.04 MHz) | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Decimation ratio | 1 | 2 | 4 | 8 | 16 | 32 | 64 | 128 | 256 | 512 |
| Output sample rate (MHz) | 23.04 | 11.52 | 5.76 | 2.88 | 1.44 | 0.72 | 0.36 | 0.18 | 0.09 | 0.045 |
| Total delay (µs) | 2.34 | 3.32 | 5.10 | 8.66 | 15.43 | 28.97 | 56.05 | 110.22 | 218.55 | 435.22 |

## Get LVDS Data Delay

To see the latency for any setup, use the function *af3030_getLvdsDataDelay*. This returns the delay in µs between RF/IF input and the corresponding LVDS data output at the LVDS connector for the current settings.

# Data timing for UMTS modulation mode and decimation ratio of 2

The ADC in the module is clocked at a rate of 61.44 Ms/s. The soft front panel allows both the modulation mode and the decimation ratio to be selected. IQSELECT_OUT is toggled only when an IQ data pair is being transmitted. If UMTS is selected as the modulation mode, the IQ sample rate is resampled and output at UMTS x 16. If a decimation rate of two is selected, the IQ data rate is 30.72 Ms/s. When configured in this way, the timing relationships for the DATA interface are as shown in Fig. A-3.
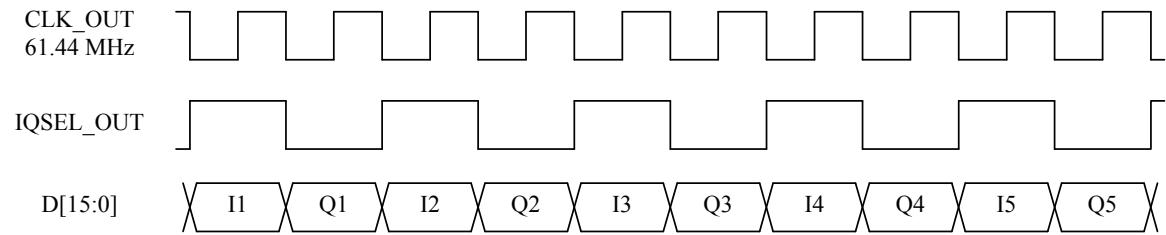


*Fig. A-3  DATA timing for UMTS mode and decimate by 2*

## Latency

The digitizer converts an analog RF waveform presented at its RF port into a series of digital IQ data pairs at its LVDS port. LVDS latency is the time taken for any given point on the input RF waveform to appear as an IQ data pair on the LVDS output. The table below lists the LVDS latency times for different IQ sample rates.

| UMTS (61.44 MHz) | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Decimation ratio | 2 | 4 | 8 | 16 | 32 | 64 | 128 | 256 | 512 | 1024 |
| Output sample rate (MHz) | 30.72 | 15.36 | 7.68 | 3.84 | 1.92 | 0.96 | 0.48 | 0.24 | 0.12 | 0.06 |
| Total delay (µs) | 2.20 | 2.93 | 4.26 | 6.93 | 12.01 | 22.17 | 42.48 | 83.10 | 164.35 | 326.85 |

# Data timing for UMTS modulation mode and decimation ratio of 4

The timing relationships for the DATA interface are as shown in Fig. A-4. The CLK_OUT signal is continuous and remains fixed at 61.44 MHz, irrespective of the modulation mode and the decimation rate. IQSELECT_OUT is toggled only when an IQ data pair is being transmitted.
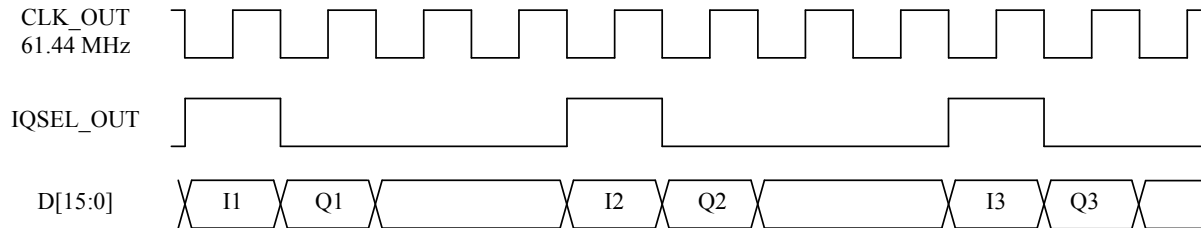


*Fig. A-4  DATA timing for UMTS mode and decimate by 4*

# Data timing for UMTS modulation mode and decimation ratio of 8

The timing relationships for the DATA interface are as shown in Fig. A-5. The CLK_OUT signal is continuous and remains fixed at 61.44 MHz, irrespective of the modulation mode and the decimation rate. IQSELECT_OUT is toggled only when an IQ data pair is being transmitted.
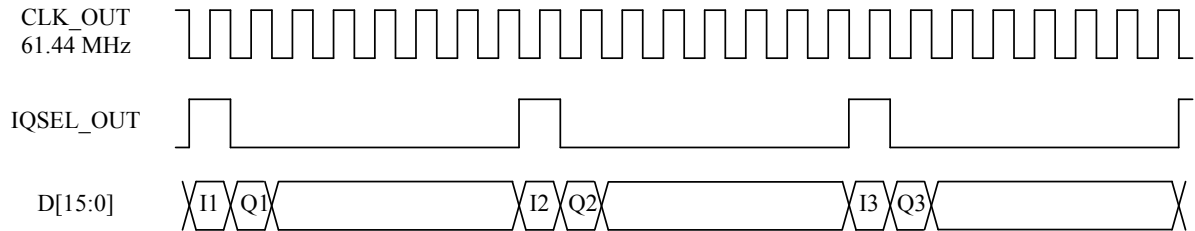


*Fig. A-5  DATA timing for UMTS mode and decimate by 8*

In addition, for decimation ratios of 8 or greater, IQ data can be 32-bit. In this mode, data is transmitted as two 16-bit words, MSW then LSW for I then Q, as shown in Fig. A-6.
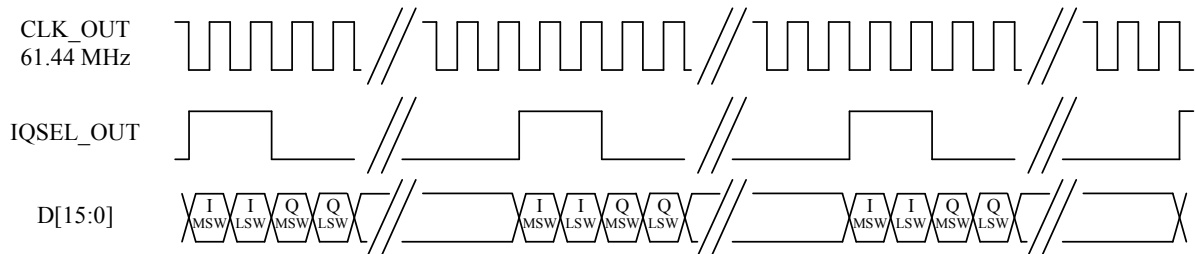


*Fig. A-6  DATA timing for 32 bit IQ, UMTS mode and decimate by 8*

# Data timing for CDMA2000 1X modulation mode

If a modulation mode of CDMA2000 1X and a decimation value of 1 are both selected, IQ data is generated at eight times the CDMA2000 1X chip rate. As the chip rate is 1.2288 MHz, this gives an IQ sample rate of 9.8304 Ms/s. There is no longer an integer relationship between the clock rate of 61.44 MHz and the 9.8304 Ms/s data rate.

The number of clock cycles between IQSELECT_OUT being asserted is not fixed but varies. This is true for all CDMA mode decimation ratios.

The timing relationship for the DATA interface is shown in Fig. A-7. Note that the CLK_OUT signal is continuous and remains fixed at 61.44 MHz, irrespective of the modulation mode and the decimation rate. IQSELECT_OUT is toggled only when an IQ data pair is being transmitted.



*Fig. A-7  DATA timing for CDMA2000 1X*

# Latency

The digitizer converts an analog RF waveform presented at its RF port into a series of digital IQ data pairs at its LVDS port. LVDS latency is the time taken for any given point on the input RF waveform to appear as an IQ data pair on the LVDS output. The table below lists the LVDS latency times, calculated for different IQ sample rates.

| CDMA2000-1x (9.8304 MHz) | | | | |
|---|---|---|---|---|
| Decimation ratio | 1 | 2 | 4 | 8 |
| Output sample rate (MHz) | 9.8304 | 4.9152 | 2.4576 | 1.2288 |
| Total delay (µs) | 3.59 | 5.67 | 9.84 | 17.78 |

# Data transmission for GSM modulation mode and a decimation ratio of 1

In this mode, the IQ data is resampled to produce IQ data at 16 times the GSM symbol rate of 270.83 kHz, that is, 4.333 Ms/s. The timing relationships for the DATA interface is as shown in Fig. A-8. Note that the CLK_OUT signal is continuous and that the frequency of the clock remains fixed at 61.44 MHz. IQSELECT_OUT is toggled only when an IQ data pair is being transmitted.

There is no longer an integer relationship between the data rate of 4.33 MHz and the clock frequency of 61.44 MHz. Therefore the number of clock cycles between IQSELECT_OUT being asserted is no longer fixed but varies. This is true for all GSM mode decimation ratios.
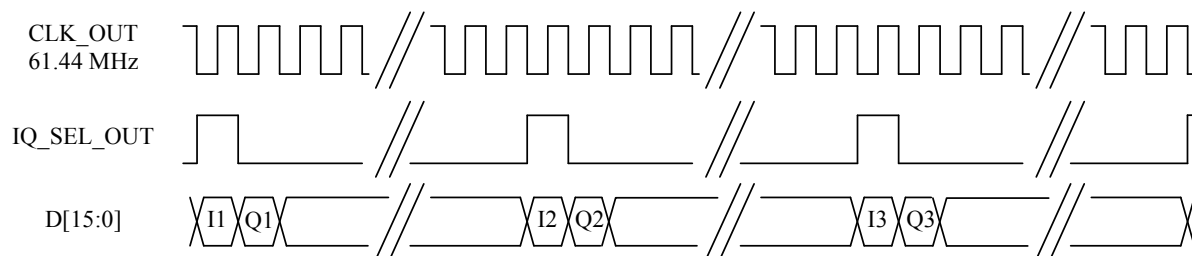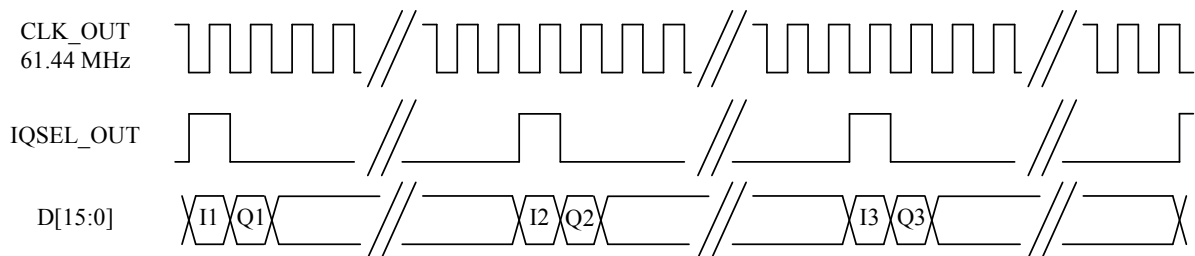


*Fig. A-8  DATA timing for GSM*

## Latency

The digitizer converts an analog RF waveform presented at its RF port into a series of digital IQ data pairs at its LVDS port. LVDS latency is the time taken for any given point on the input RF waveform to appear as an IQ data pair on the LVDS output. The table below lists the LVDS latency times, calculated for different IQ sample rates.

| GSM (4.333333 MHz) | | | | | |
|---|---|---|---|---|---|
| Decimation ratio | 1 | 2 | 4 | 8 | 16 |
| Output sample rate (MHz) | 4.333333 | 2.166667 | 1.083333 | 0.541667 | 0.270833 |
| Total delay (µs) | 6.20 | 10.93 | 19.93 | 37.93 | 79.93 |

# Data transmission for 2319E emulation mode

In this mode, the IQ data is resampled to produce IQ data at 4.08 MHz with a decimation ratio of 16. The timing relationships for the DATA interface are as shown in Fig. A-9. Note that the CLK_OUT signal is continuous and that the frequency of the clock remains fixed at 61.44 MHz. IQSELECT_OUT is toggled only when an IQ data pair is being transmitted.

There is no integer relationship between the data rate of 4.08 MHz and the clock frequency of 61.44 MHz. Therefore the number of clock cycles between IQSELECT_OUT being asserted is no longer fixed but varies. This is true for all 2319E modulation mode decimation ratios.
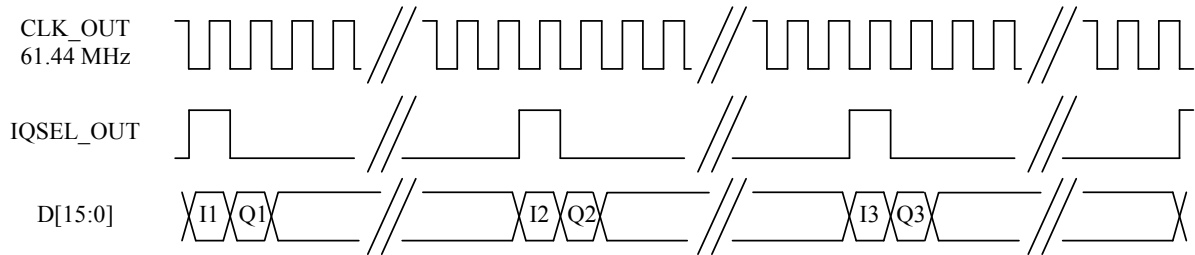


*Fig. A-9  DATA timing for 2319E emulation*

## Latency

The digitizer converts an analog RF waveform presented at its RF port into a series of digital IQ data pairs at its LVDS port. LVDS latency is the time taken for any given point on the input RF waveform to appear as an IQ data pair on the LVDS output. The table below lists the LVDS latency times, calculated for different IQ sample rates.

| 2319E emulation (65.28 MHz) | | |
|---|---|---|
| Decimation ratio | 16 | 32 |
| Output sample rate (MHz) | 4.08 | 2.04 |
| Total delay (µs) | 6.48 | 11.50 |

# Data transmission in IF data format

In IF data format, the IQ_SELECT signal remains low and IF data is clocked on each ADC clock cycle at a fixed sample rate of 61.44 MHz

## Latency

LVDS latency in IF data format is the time taken for any given point on the input RF waveform to appear as an IF data on the LVDS output.

| IF (61.44 MHz) | |
|---|---|
| Total delay (µs) | 1.33 |

# Chapter 4 BRIEF TECHNICAL DESCRIPTION

## Introduction

3030 is a PXI RF bandpass digitizer, digitizing an instantaneous IF bandwidth of 20 MHz with a 14-bit converter. Digitized RF can be stored in a large internal RAM and read back over PXI. It can also be streamed out of a front panel LVDS output at full speed. Flexible signal and trigger processing is available.

3030 can be operated as a spectrum analyzer, modulation analyzer, demodulator or part of a radio test set, by selecting the appropriate application software.

3030 is a three-board design occupying two slots in the backplane. The first board is a single stage RF downconverter to IF, with an input attenuator and output gain. It must be used with an external LO from a 3010 RF Synthesizer module or other RF source. The IF output is normally linked externally to the second board, which digitizes the input IF signal. It has switchable input gain, an anti-alias filter with bypass and a clock source. It outputs data to the third board, which provides all of the digital services required by the module, including the power supply, PXI interface, LVDS interface, memory and digital signal processing. A block schematic for the instrument is shown in Fig. 4-1.

# RF board

The input attenuator has three pads, which provide 2 dB of loss in the 'thru' condition, and 6, 10 and 18 dB of loss respectively in the 'attenuate' condition, giving 28 dB of control in 4 dB steps.

The 3010 RF Synthesizer generates a top octave of 1500 MHz to 3 GHz. This is amplified to provide level control, then split to the RF switch and to the dividers. It is divided down for frequencies below 1500 MHz. The signal is switched through up to two dividers in cascade and then amplified to +17 dBm before application to the mixer, which has an input frequency range of 330 MHz to 3 GHz.

The mixer is followed by a diplexing filter, which provides a good broadband match and low-pass filters the IF output, and a 10 dB gain amplifier. The loss of the mixer, its excess noise, the loss of the diplexing filter and the noise figure of the amplifier define the noise floor of the downconverter system.

# IF board

The signal is input to an IF amplifier of adjustable gain. The IF amplifier consists of three 10 dB gain stages, with switchable pads. They provide a maximum gain of 30 dB, and a minimum gain of –5 dB.

The signal then enters an anti-alias bandpass filter, which passes signals at 75% of the digitizer sampling rate. This can be bypassed if required. The ADC sample rate is generated from a VCXO, which is phase locked to the 10 MHz signal relayed from the downconverter board. The ADC outputs are buffered and sent to the logic board.

# Digital board

The logic board has several functions: an interface to the PCI bus, digital signal processing of IF data, data capture memory management, control of the LVDS data interface, and serial control of the digitizer and downconverter boards.

The PCI interface uses an FPGA, which boots up at power-on from flash memory, and which controls the logic on the board and in the rest of the module via serial links.

Another FPGA provides all of the signal processing hardware, and can be reloaded as the data processing is required to change.  The data path from the ADC is first corrected for frequency response by an FIR filter.  This corrects for the amplitude and group delay non-flatness created by the anti-alias filter.  The data is then downconverted to I and Q using a complex mix, and decimated to a lower data rate consistent with the modulation bandwidth.  Finally, the data is optionally resampled to another clock rate appropriate to the data rate of the modulation.  Alternatively all processing can be bypassed to capture raw IF data.

A 64-bit memory module is used to capture data.  The SDRAM controller allows continuous sample-rate capture of IQ or IF data being written into SDRAM, or 32-bit PCI burst transfers for reading data from SDRAM to controller memory.  Simultaneous writing and reading of memory is not possible.

IF or IQ data can also be routed to an external LVDS data interface.  This uses bidirectional transceivers for maximum flexibility, with clock in and out, 16-bit data, IQ select for multiplexed data, 4-bit markers, 5-bit auxiliary signals and spare lines.
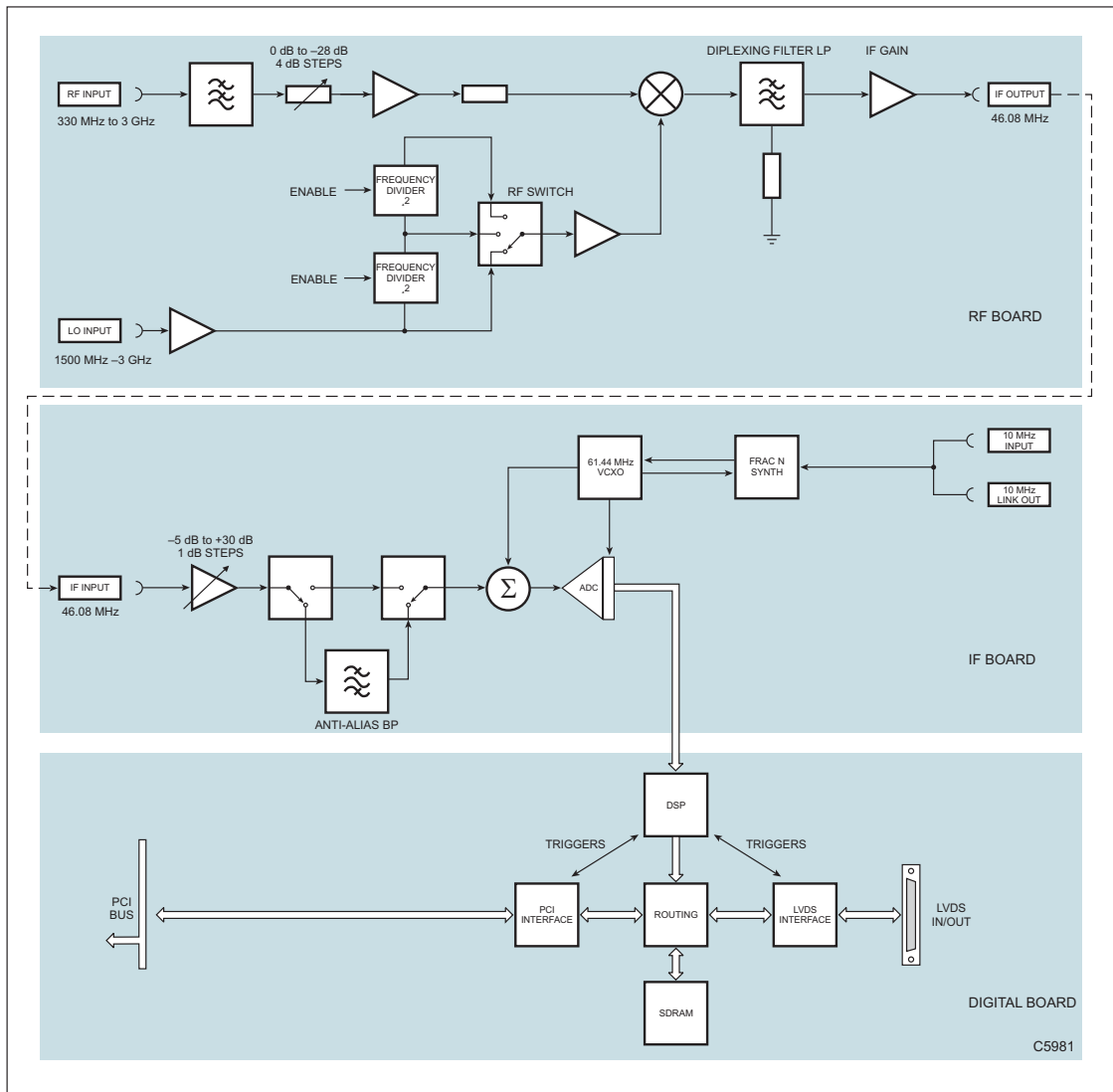
*Fig. 4-1  Block schematic diagram*

# Chapter 5 ACCEPTANCE TESTING

## Introduction

The test procedures in this chapter enable you to verify that the 3030 RF Digitizer module is meeting its specified performance.

## Abbreviations

Throughout the chapter, the following abbreviations are used:

UUT     Unit Under Test
SFP     Soft Front Panel

## Test procedures

Each test procedure shows you how to configure the test equipment and then describes how to perform the test. Tables are provided for recording your results. Measurements should fall within the maximum and minimum limits indicated, provided that you use the recommended test equipment and adhere to the test precautions.

The tests recommend the use of conventional 'rack and stack' test equipment, apart from the LO for the 3030 UUT, where an Aeroflex 3011 RF synthesizer is specified. Other PXI modules may be used as long as they comply with the minimum specification.

# Controlling the UUT

Control the UUT with the RF Investigator SFP, which is on the supplied CD−ROM (part no. 46886/028) as part of the common installation.

Follow the instructions provided in the 3000 Series Common Installation Guide (part no. 46882/663) to ensure that this software is correctly installed.

Each test procedure relies on the module being set to its power−up conditions.  To avoid switching the PXI chassis off and back on, close and restart the RF Investigator SFP, then boot the module.

*Note that for clarity, the PXI chassis and controller are not shown in the setup diagrams for the test equipment.*

# Recommended test equipment

The test equipment recommended is shown below.  You may use alternative equipment provided it complies with the stated minimum specification.  The minimum specification is only an indication of the required performance.  With all measurements, you should ensure that the performance of the test equipment has adequate stand–off from the specification of the UUT.

| Description | Minimum specification | Example | Test parameters |
|---|---|---|---|
| Signal generator | 330 MHz to 3 GHz<br><br>Arbitrary waveform generator | Aeroflex 3413 with Options 5 and 21 | RF level accuracy<br>ACLR |
| PXI synthesizer | 1.5 GHz to 3 GHz | Aeroflex 3011 | Local oscillator |
| Power meter and sensor | 330 MHz to 3 GHz | Aeroflex 6960B and 6912 | RF level accuracy |
| Power splitter | 3 GHz | Agilent 11667B | RF level accuracy |
| Microwave scalar analyzer | 330 MHz to 3 GHz | Aeroflex 6821, 6822 or 6823 | RF Input return loss |
| Autotester | 330 MHz to 3 GHz | Aeroflex 59999/168 | RF Input return loss |
| 50 ohm SMA termination | 330 MHz to 3 GHz | Aeroflex 82532 | Residual responses / noise spectral density |
| Oscilloscope | 10 MHz | Tektronix TDS3032 | 10 MHz reference output |

# Test precautions

To ensure minimum errors and uncertainties when making measurements, it is important to observe the following precautions:

- Always use recently calibrated test equipment, with any correction figures taken into account, to establish a known traceable limit of performance uncertainty. This uncertainty must be allowed for in determining the accuracy of measurements.

- Ensure any user calibration routines are performed when necessary. On most power meters, it is also necessary to perform an auto-zero routine.

- Use the shortest possible connecting leads.

- Allow 20 minutes for the UUT to warm up, plus any extra time for other test equipment being used.

# Checking that the UUT powers up correctly

This test ensures that the module powers up in a satisfactory manner and that the internal self-tests do not report any errors. This test assumes that the module is fitted in a PXI chassis and that the necessary supplied software is installed on the host controller.

- Apply power to the PXI chassis.
- Press the supply switch on the PXI chassis.

Wait for the operating system to complete its boot-up sequence.

- Click on *Start\Programs\Aeroflex\RF Investigator*.

Boot the module via the SFP as follows:

- Click on *File\Resource\[Dig]*.
- After a few seconds, the appropriate indicators turn green to show that the boot sequence has completed successfully.
- Click **OK**.

# Level accuracy test

This test measures the RF level accuracy across the frequency range of the instrument at a selection of RF attenuator and IF attenuator settings. The first two sets of values recorded are with the RF attenuation fixed at 16dB with minimum (0 dB), then maximum (35 dB), IF attenuation. The second two sets of values recorded are with the IF attenuation fixed at 12 dB with minimum (4 dB), then maximum (28 dB) RF attenuation.
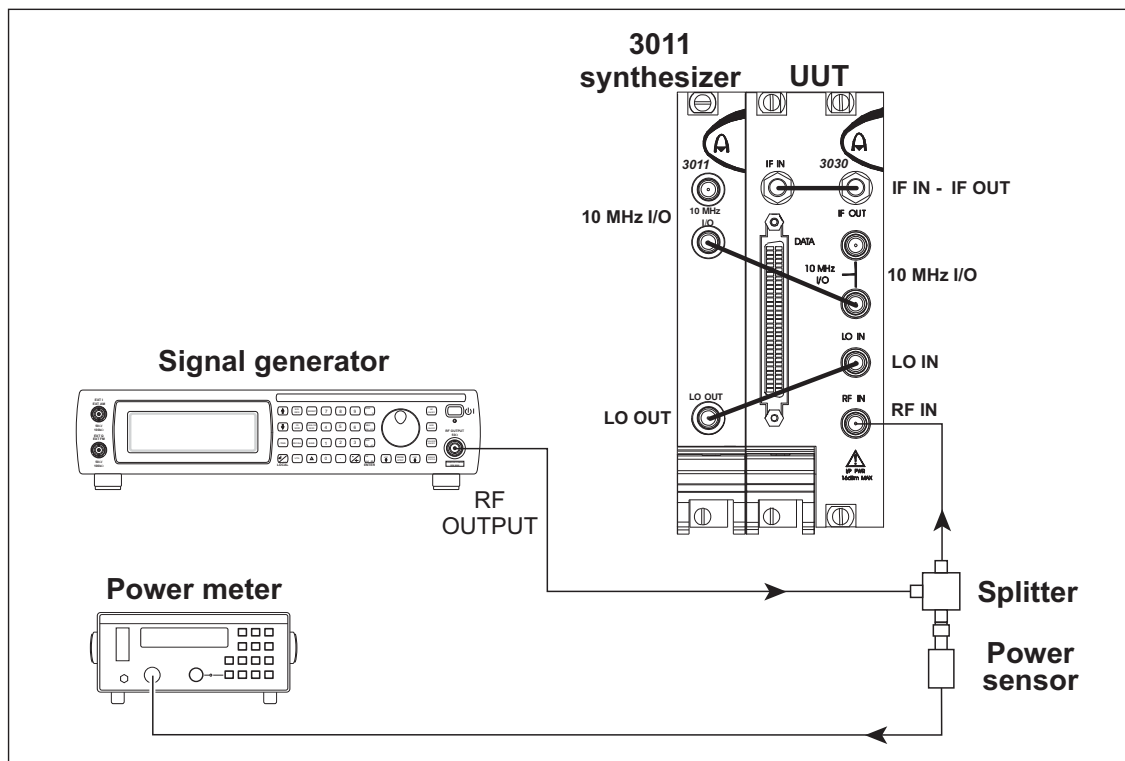


C5943

*Fig. 5-1  Level accuracy test setup*

1    Connect the test equipment as shown in Fig. 5-1.

2    On the signal generator set:

| | |
|---|---|
| Carrier Frequency | 330 MHz |
| RF Level | 0 dBm |

3    On the UUT set:

| | |
|---|---|
| Centre Frequency (MHz) | 330.000000 |
| RF Level (dBm) | 10 |
| RF Atten (dB) | 16 |
| IF Atten (dB) | 0 |
| Trace Mkr | click check box |

Hint: right-click on **Centre Frequency (MHz)** and set a frequency step of 250 MHz. From the 500 MHz frequency upwards, this will speed up the test. Set a 250 MHz step on the signal generator also.

4    On the UUT:
click on **Single**, then **Peak**
Read the Mkr. level at the top of the display and record the value in Table 5-1 column a.

5    Read the level displayed on the power meter and record the value in Table 5-1 column b.

6    Record the error in Table 5-1 column c.        (c = a – b)

7    Repeat (4) to (6) for the remaining frequencies in Table 5-1, setting the UUT and signal generator frequencies as necessary.

8    On the UUT set:

| | |
|---|---|
| IF Atten | 35 |

9    Repeat (4) to (6) using Table 5-2.

10  On the UUT set:

| | |
|---|---|
| RF Atten (dB) | 4 |
| IF Atten (dB) | 12 |

11  Repeat (4) to (6) using Table 5-3.

12  On the UUT set:

RF Atten (dB)                    28

13  Repeat (4) to (6) using Table 5-4.

**Table 5-1  Amplitude accuracy with 16 dB input atten. and 0 dB IF atten.**

| Frequency (MHz) | UUT display level (dBm) a | Power meter reading (dBm) b | Error (dBm) c | Limit (dBm) |
|---|---|---|---|---|
| 330 | | | | ±0.6 |
| 500 | | | | ±0.6 |
| 750 | | | | ±0.6 |
| 1000 | | | | ±0.6 |
| 1250 | | | | ±0.6 |
| 1500 | | | | ±0.6 |
| 1750 | | | | ±0.6 |
| 2000 | | | | ±0.6 |
| 2250 | | | | ±0.6 |
| 2500 | | | | ±0.6 |
| 2750 | | | | ±0.6 |
| 3000 | | | | ±0.6 |

**Table 5-2  Amplitude accuracy with 16 dB input atten. and 35 dB IF atten.**

| Frequency (MHz) | UUT display level (dBm) | Power meter reading (dBm) | Error (dBm) | Limit (dBm) |
|---|---|---|---|---|
| | a | b | c | |
| 330 | | | | ±0.6 |
| 500 | | | | ±0.6 |
| 750 | | | | ±0.6 |
| 1000 | | | | ±0.6 |
| 1250 | | | | ±0.6 |
| 1500 | | | | ±0.6 |
| 1750 | | | | ±0.6 |
| 2000 | | | | ±0.6 |
| 2250 | | | | ±0.6 |
| 2500 | | | | ±0.6 |
| 2750 | | | | ±0.6 |
| 3000 | | | | ±0.6 |

**Table 5-3  Amplitude accuracy with 4 dB input atten. and 12 dB IF atten.**

| Frequency (MHz) | UUT display level (dBm) a | Power meter reading (dBm) b | Error (dBm) c | Limit (dBm) |
|---|---|---|---|---|
| 330 | | | | ±0.6 |
| 500 | | | | ±0.6 |
| 750 | | | | ±0.6 |
| 1000 | | | | ±0.6 |
| 1250 | | | | ±0.6 |
| 1500 | | | | ±0.6 |
| 1750 | | | | ±0.6 |
| 2000 | | | | ±0.6 |
| 2250 | | | | ±0.6 |
| 2500 | | | | ±0.6 |
| 2750 | | | | ±0.6 |
| 3000 | | | | ±0.6 |
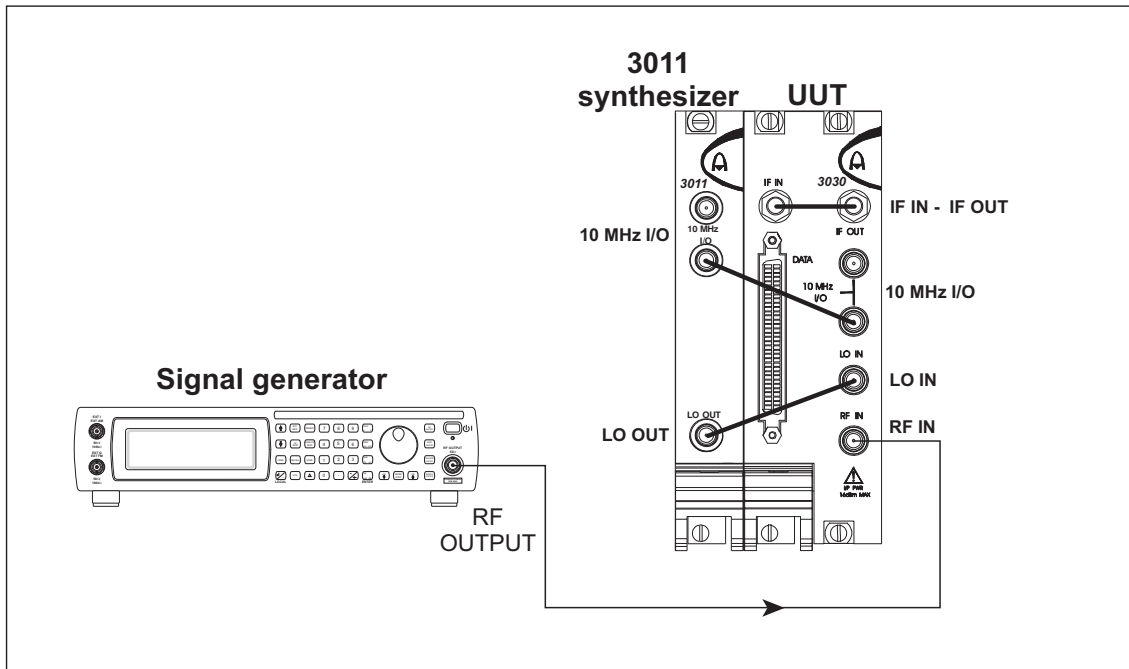
**Table 5-4  Amplitude accuracy with 28 dB input atten. and 12 dB IF atten.**

| Frequency (MHz) | UUT display level (dBm) a | Power meter reading (dBm) b | Error (dBm) c | Limit (dBm) |
|---|---|---|---|---|
| 330 | | | | ±0.6 |
| 500 | | | | ±0.6 |
| 750 | | | | ±0.6 |
| 1000 | | | | ±0.6 |
| 1250 | | | | ±0.6 |
| 1500 | | | | ±0.6 |
| 1750 | | | | ±0.6 |
| 2000 | | | | ±0.6 |
| 2250 | | | | ±0.6 |
| 2500 | | | | ±0.6 |
| 2750 | | | | ±0.6 |
| 3000 | | | | ±0.6 |

# Linearity and noise

## Adjacent channel leakage ratio (ACLR)

Load the signal generator's arbitrary waveform generator with the 3GPP, 64-channel, test model 1, downlink example test waveform: *ats_3gpp_fdd_fwd_tm1_64ch_sc0_v5pt1.aiq.*



*Fig. 5-2  ACLR test setup*

1    Connect the test equipment as shown in Fig. 5-2.

2    On the signal generator set:

| Carrier Frequency | 330 MHz |
|---|---|
| RF Level | 0 dBm |

Select and play the waveform:
*ats_3gpp_fdd_fwd_tm1_64ch_sc0_v5pt1.aiq*

3    On the UUT set:

| Carrier Frequency (MHz) | 330.000000 |
|---|---|
| RF Level (dBm) | 0 |
| RF Atten | 12[1] |
| IF Atten | 15[1] |
| ACP | click check box |

From the toolbar, click on *Config\Spectrum Analyser* and check that the following parameters are set:

| Analysis Width (MHz) | 20 |
|---|---|
| Percentage | 99.00 |
| Centre Freq (MHz) | 0 |
| Channel Spacing (MHz) | 5.00 |
| Channel Width (MHz) | 3.84 |
| Alpha | 0.22 |

Click **OK**.

4    On the UUT:

Click on **Single**.
Read the upper and lower adjacent channel power values and record them in Table 5-5.

5    Repeat (2) to (4) for the remaining frequencies in Table 5-5, setting the UUT and signal generator frequencies as necessary.

---

[1] It may be necessary to adjust the input attenuation and/or the IF attenuation to achieve best results. Do not allow the A2D indicator to turn red as this indicates a front-end overload.

**Table 5-5  ACLR results**

| Frequency (MHz) | 1<sup>st</sup> lower (dBc) | 1<sup>st</sup> upper (dBc) | Limit (dBc) |
|---|---|---|---|
| 330 | | | <−63 |
| 400 | | | <−63 |
| 800 | | | <−63 |
| 1200 | | | <−63 |
| 1600 | | | <−63 |
| 2000 | | | <−63 |
| 2400 | | | <−63 |
| 2800 | | | <−63 |
| 3000 | | | <−63 |

# Residual responses

No test equipment is required.

1    On the UUT, connect a 50 ohm termination to the RF IN connector.

2    On the UUT set:

| | |
|---|---|
| Centre Frequency (MHz) | 340.000000 |
| Step Size | 20 MHz |
| Ref Level (dBm) | −70 |
| Span (MHz) | 20 |
| NBW (kHz) | 10.0 |
| RF Atten | 0 |
| IF Atten | 0 |
| Averaging | 10 |
| Trace Mkr | click check box |

3    On the UUT:

Click on **Single**, then **Peak**.

4    Check the displayed trace for any residual responses.  Increase Centre Frequency in 20 MHz steps up to 3000 MHz using the Centre Frequency increment icon, and repeat (3) above, waiting briefly for the sweep averaging to complete.  Record the level and frequency of the largest residual responses, if any are found, in Table 5-6.

## Table 5-6  Residual responses results

| Frequency (MHz) | Result (dBm) | Limit (dBm) |
|---|---|---|
|  |  | −100 |
|  |  | −100 |
|  |  | −100 |
|  |  | −100 |
|  |  | −100 |
|  |  | −100 |
|  |  | −100 |
|  |  | −100 |

# Noise spectral density

No test equipment is required.

1   On the UUT, connect a 50 ohm termination to the RF IN connector.

2   On the UUT set:

| | |
|---|---|
| Centre Frequency (MHz) | 330.000000 |
| Step Size | 100 MHz |
| Ref Level (dBm) | –70 |
| Span (MHz) | 20 |
| NBW (kHz) | 10.0 |
| RF Atten | 0 |
| IF Atten | 0 |
| Averaging | 50 |
| Trace Mkr | click check box |

3   On the UUT:

Click on **Single**, then **Peak**.

It may be necessary to drag the marker off any residual response as this gives a false indication of the noise floor.  Subtract 40 dB from the Mkr. level at the top of the display (to normalize to a 1 Hz bandwidth) and record the value in Table 5-7
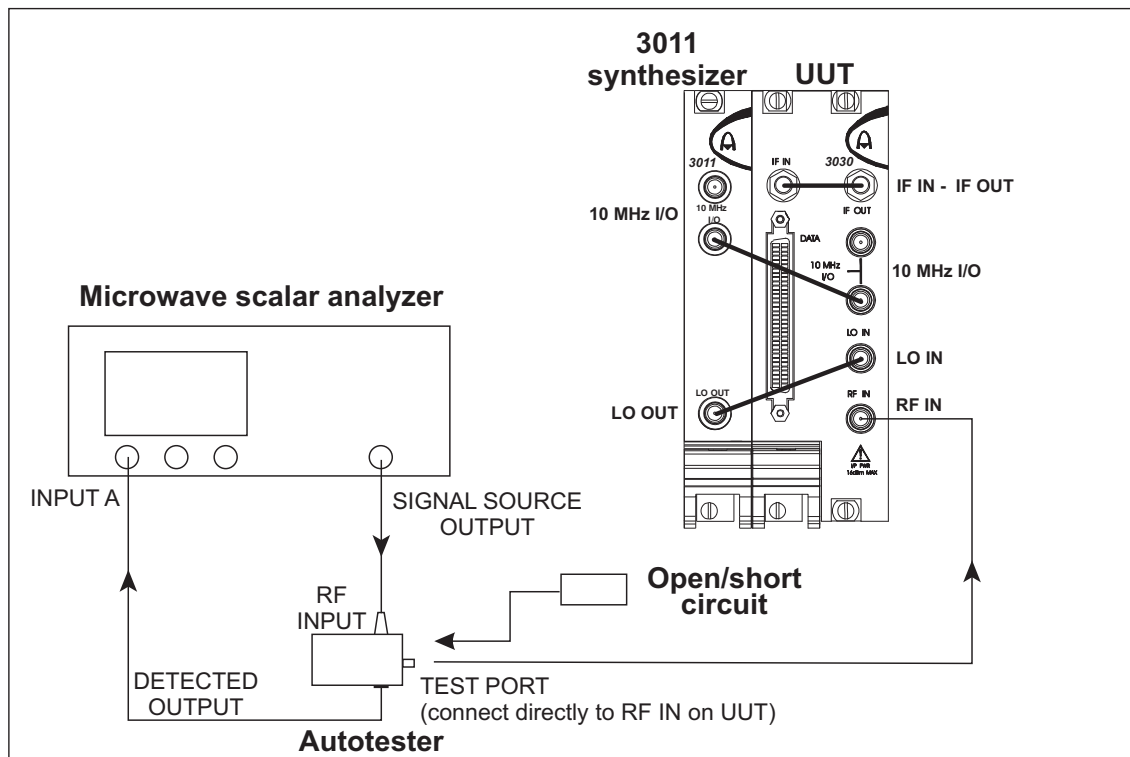
4   Repeat (3) for each of the frequencies shown in Table 5-7, using the Centre Frequency increment icon where appropriate.

**Table 5-7  Noise spectral density results**

| Frequency (MHz) | Result (dBm) | Limit (dBm) |
|---|---|---|
| 330 | | −140 |
| 400 | | −140 |
| 600 | | −140 |
| 800 | | −140 |
| 999 | | −140 |
| 1000 | | −140 |
| 1200 | | −140 |
| 1400 | | −140 |
| 1600 | | −140 |
| 1800 | | −140 |
| 2000 | | −140 |
| 2100 | | −140 |
| 2200 | | −140 |
| 2300 | | −140 |
| 2400 | | −140 |
| 2500 | | −140 |
| 2600 | | −140 |
| 2700 | | −140 |
| 2800 | | −140 |
| 2900 | | −140 |
| 3000 | | −140 |

# RF input return loss



*Fig. 5-3  RF input VSWR test setup*

1   Connect the test equipment as shown in Fig. 5-3.

2   On the UUT set:

| RF Level (dBm) | 0 |
| RF Atten | 8 |
| IF Atten | 15 |

3    On the Microwave Scalar Analyzer (MSA) define the source conditions as follows:

[PRESET]
*[Full]*
[SOURCE]
*[Set Start Frequency]*          330 [Mu]
*[Set Stop Frequency]*          3 [Gn]

4    Calibrate the MSA for VSWR measurements as follows:

[CAL]
*[Short AND Open Cal]*

5    Connect the short-circuit to the test port of the autotester.

6    On the MSA select *[Continue]*

7    Remove the short-circuit and connect the open-circuit to the test port of the autotester.

8    On the MSA select *[Continue]*

9    Remove the open-circuit and connect the test port of the autotester directly to the UUT's RF IN input.

10  On the MSA select:

[FORMAT/SCALING]
*[VSWR]*

Using the rotary control on the MSA, measure the worst-case return loss and record the frequency and value in Table 5-8.

**Table 5-8  RF input return loss result**

| Frequency (MHz) | Result (dB) | Limit (dB) |
|---|---|---|
|  |  | 16 dB |

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9.3  On termination of this Agreement for any reason, Aeroflex may require the Licensee to return to Aeroflex all copies of the Licensed Software in the custody of the Licensee and the Licensee shall, at its own cost and expense, comply with such requirement within 14 days and shall, at the same time, certify to Aeroflex in writing that all copies of the Licensed Software in whatever form have been obliterated from the Designated Equipment.

## 10.  THIRD PARTY LICENCES

The software or part thereof may be the proprietary property of third party licensors. In such an event such third party licensors (as referenced on the package or the Order Acknowledgement) and/or Aeroflex may directly enforce the terms of this Agreement and may terminate the Agreement if the Licensee is in breach of the conditions contained herein.

## 11.  EXPORT REGULATIONS

The Licensee undertakes that where necessary the Licensee will conform with all relevant export regulations imposed by the Governments of the United Kingdom and/or the United State of America.

## 12.  NOTICES

Any notice to be given by the Licensee to Aeroflex shall be addressed to:

Aeroflex International Limited, Longacres House, Six Hills Way, Stevenage, SG1 2AN, UK.

**13. LAW AND JURISDICTION**

This Agreement shall be governed by the laws of England and shall be subject to the exclusive jurisdiction of the English courts.  This agreement constitutes the whole Contract between the parties and may be changed only by memorandum signed by both parties.

*As we are always seeking to improve our products, the information in this document gives only a general indication of the product capacity, performance and suitability,none of which shall form part of any contract.  We reserve the right to make design changes without notice.*

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